

9097248 TOSHIBA (LOGIC/MEMORY)

CCD LINEAR IMAGE SENSOR
 CCD (Charge Coupled Device)

TCD103C

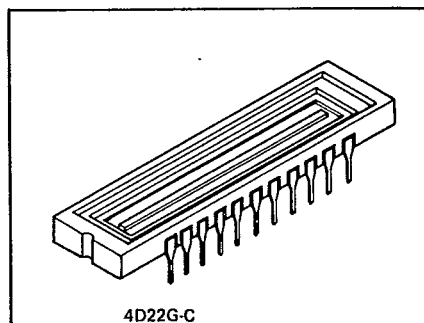
67C 09531 D T-41-55

The TCD103C is a high resolution and high sensitivity 2592 elements linear image sensor.

The sensor is designed for Facsimile, OCR and copy M/C.

The device contains a row of 2592 photo-diodes which provide a 8 line/mm resolution across a A3 size paper, and a 12 line/mm resolution across a A4 size paper.

The device is operated by only 12V power supply, and mounted in 22 pin dual-in-line package with hermetic sealed optical glass window.



FEATURES:

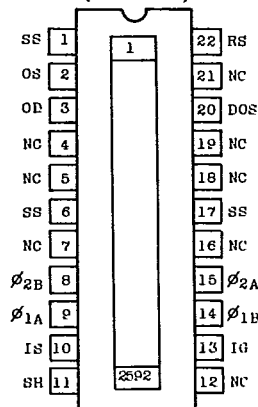
- . Number of Image Sensing Elements : 2592
- . Image Sensing Element Size : 11 μ m by 11 μ m on 11 μ m centers
- . Photo Sensing Region : High sensitive pn photodiode
- . Clock : 2 Phase
- . Dynamic Range : 600 (Typ.)
- . Package : 22 pin DIP

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V_{ϕ}	-0.3 ~ 15	V
Shift Pulse Voltage	V_{SH}		
Reset Pulse Voltage	V_{RS}		
Output Transistor Drain Voltage	V_{OD}		
Input Gate Voltage	V_{IG}		
Input Source Voltage	V_{IS}		
Operating Temperature	T_{op}		
Storage Temperature	T_{stg}	-40 ~ 100	$^{\circ}$ C

Note : All voltage are with respect to SS terminal (Ground).

**PIN CONNECTIONS
 (TOP VIEW)**

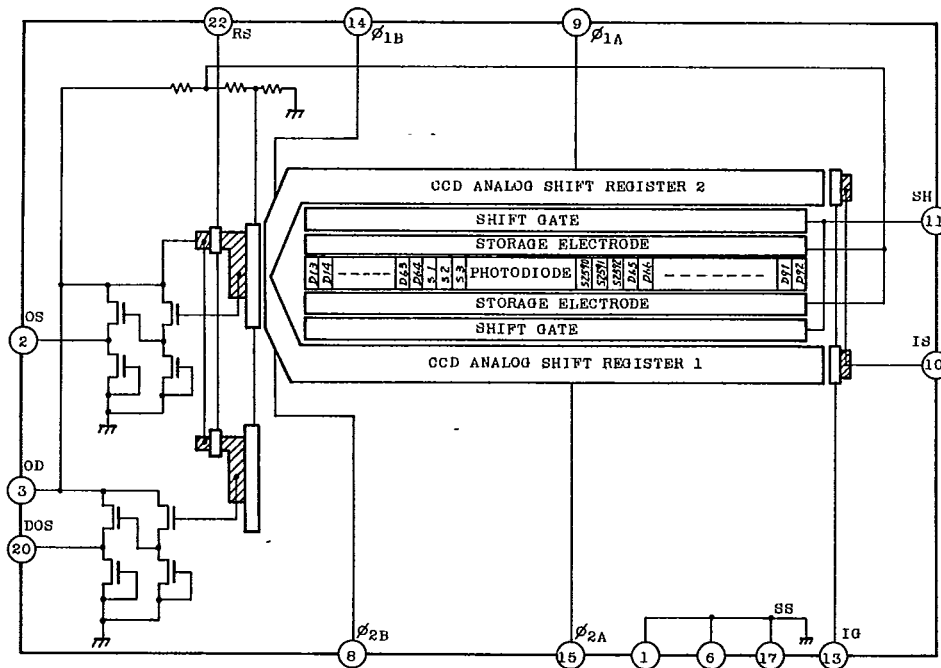


9097248 TOSHIBA (LOGIC/MEMORY)

67C 09532 D T-41-55

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CIRCUIT DIAGRAM



PIN NAMES

$\phi 1A$	Clock (Phase 1)
$\phi 2A$	Clock (Phase 2)
$\phi 1B$	Final Stage Clock (Phase 1)
$\phi 2B$	Final Stage Clock (Phase 2)
SH	Shift Gate
RS	Reset Gate
OS	Output Transistor Source
DOS	Compensation Transistor Source
OD	Output Transistor Drain
SS	Substrate (Ground)
IS	Input Source (Test Point)
IG	Input Gate (Test Point)
NC	Non Connection

9097248 TOSHIBA (LOGIC/MEMORY)

67C 09533 D T-41-55

TCD103C

OPTICAL/ELECTRICAL CHARACTERISTICS

Ta=25°C, V_{OD}=V_{IS}=12V, V_{IG}=0V, V_φ=V_{SH}=V_{RS}=12V (PULSE), f_d=0.5MHz, f_{RS}=1MHz,
t_{INT} (INTEGRATION TIME)=10msec, LIGHT SOURCE=DAYLIGHT FLUORESCENT LAMP

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Responsivity	R		0.84	1.05	1.26	V/lx·sec
Photo Response Non Uniformity	PRNU	Note (1)	-	-	±10	%
Saturation Output Voltage	V _{SAT}	V _{OD} =11.4V	0.8	1.0	-	V
Saturation Exposure	SE	V _{SAT} /R	0.63	1.05	-	lx·sec
Dark Signal Voltage	V _{DARK}	V _{OD} =13V	-	1.8	10	mV
DC Power Dissipation	P _D	V _{OD} =13V	-	100	150	mW
Total Transfer Efficiency	TTE		90	95	-	%
Output Impedance	Z _o		-	0.5	1.0	kΩ
Dynamic Range	DR	V _{SAT} /V _{DARK}	-	600	-	-
DC Mismatch Voltage	V _{OS} -V _{DOS}		-	-	300	mV

Note (1) : Measured at 50% of SE (Typ.)

PRNU is defined as follows, $PRNU = \frac{4x}{\bar{y}} \times 100 (\%)$

where \bar{y} is average of total photodiode outputs and $4x$ is deviation of photodiode output under uniform illumination.

9097248 TOSHIBA (LOGIC/MEMORY)

67C 09534 D T-41-55

TCD103C

OPERATING CONDITION (Ta=25°C)

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Voltage	H-Level	V ϕ 1A,B	11	12	13	V
	L-Level	V ϕ 2A,B	0	0.5	0.8	V
Shift Pulse Voltage	H-Level	V _{SH}	11	12	13	V
	L-Level		0	0.5	0.8	V
Reset Pulse Voltage	H-Level	V _{RS}	11	12	13	V
	L-Level		0	0.5	0.8	V
Output Transistor Drain Voltage		V _{OD}	11.4	12	13	V
Input Gate Voltage		V _{IG}	0	0	1	V
Input Source Voltage		V _{IS}	11	12	13	V

CLOCK CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f ϕ	-	0.5	-	MHz
Reset Pulse Frequency	f _{RS}	-	1.0	-	MHz
Clock Capacitance	C ϕ A	-	900	-	pF
Final Stage Clock Capacitance	C ϕ B	-	25	-	pF
Shift Gate Capacitance	C _{SH}	-	160	-	pF
Reset Gate Capacitance	C _{RS}	-	10	-	pF

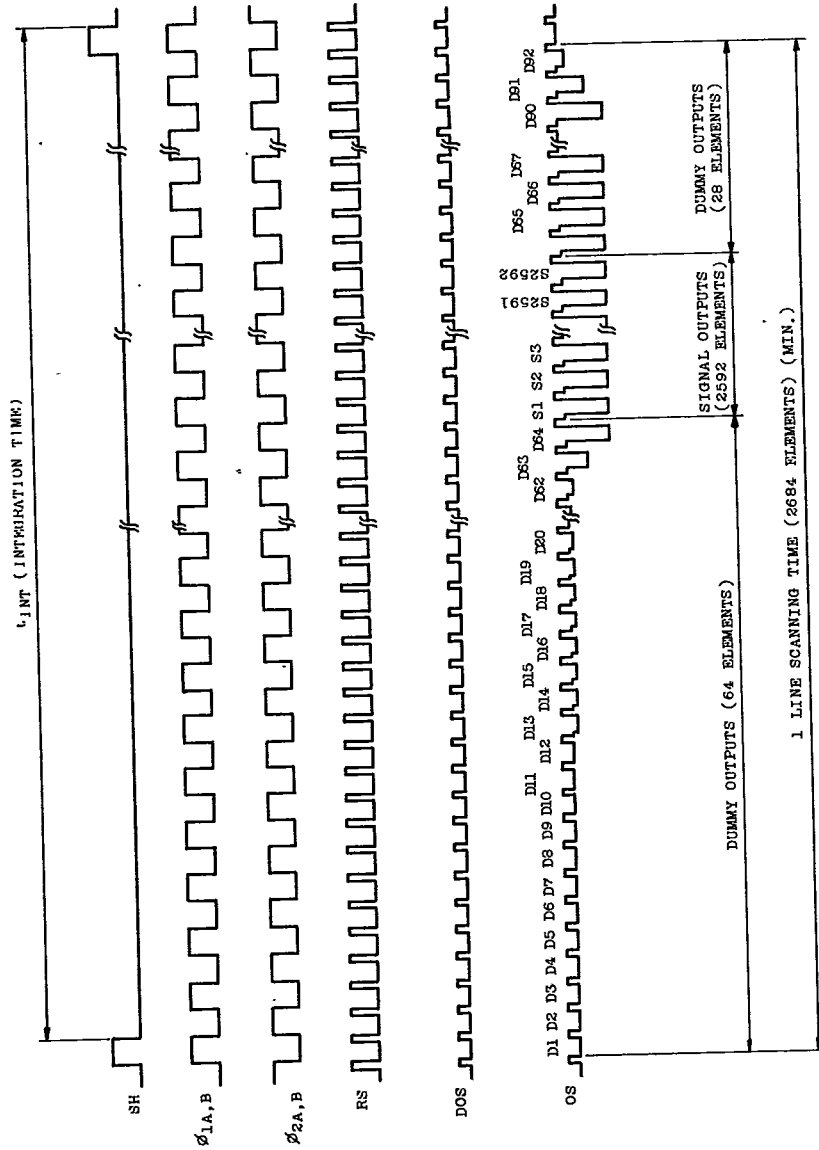
Note : You can connect electrically ϕ 1A and ϕ 1B (ϕ 1B and ϕ 2B) terminals for supplying clock pulses by one clock driver in case that f_{RS} ≤ 5MHz.

9097248 TOSHIBA (LOGIC/MEMORY)

67C 09535 D T-41-55

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TIMING CHART



9097248 TOSHIBA (LOGIC/MEMORY)

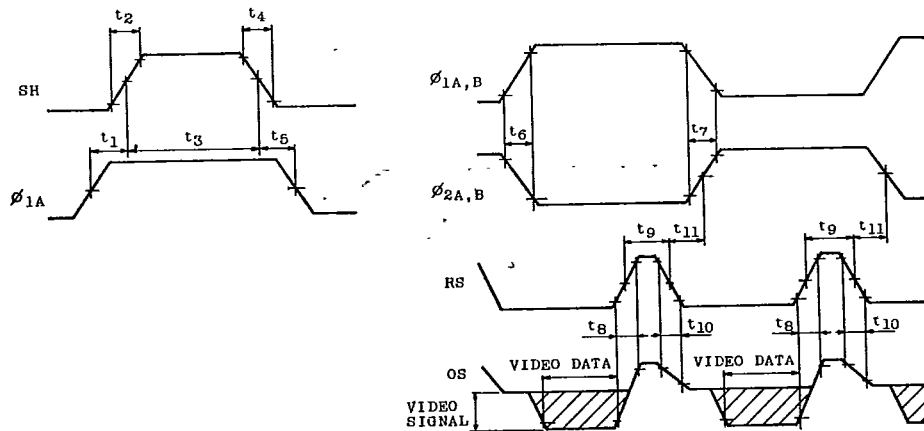
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T-41-55

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TIMING REQUIREMENTS



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Pulse Timing of SH and $\phi_{1A,B}$	t_1, t_5	0	100	-	nsec
SH Pulse Rise Time, Fall Time	t_2, t_4	0	50	-	nsec
SH Pulse Width	t_3	60	300	-	nsec
$\phi_{1A,B}$, $\phi_{2A,B}$ Pulse Rise Time, Fall Time	t_6, t_7	0	100	-	nsec
RS Pulse Rise Time, Fall Time	t_8, t_{10}	0	20	-	nsec
RS Pulse Width	t_9	30	250	-	nsec
Pulse Timing of $\phi_{1A,B}$, $\phi_{2A,B}$ and RS	t_{11}	0	250	-	nsec

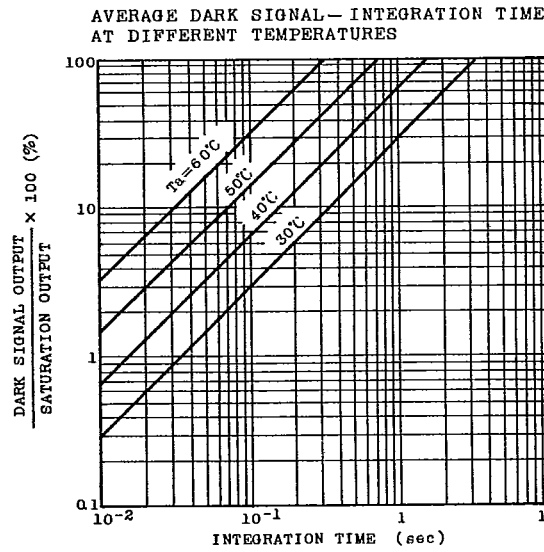
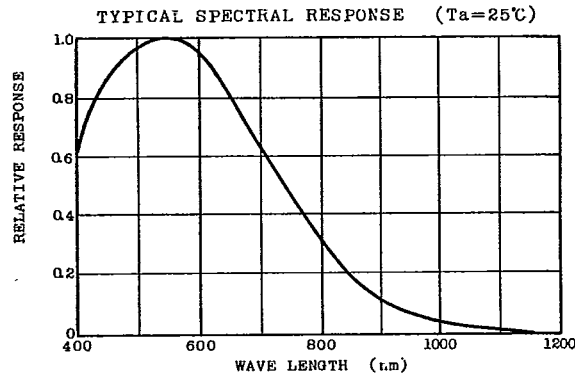
Note : $f_{RS}=1\text{MHz(Typ.)}$

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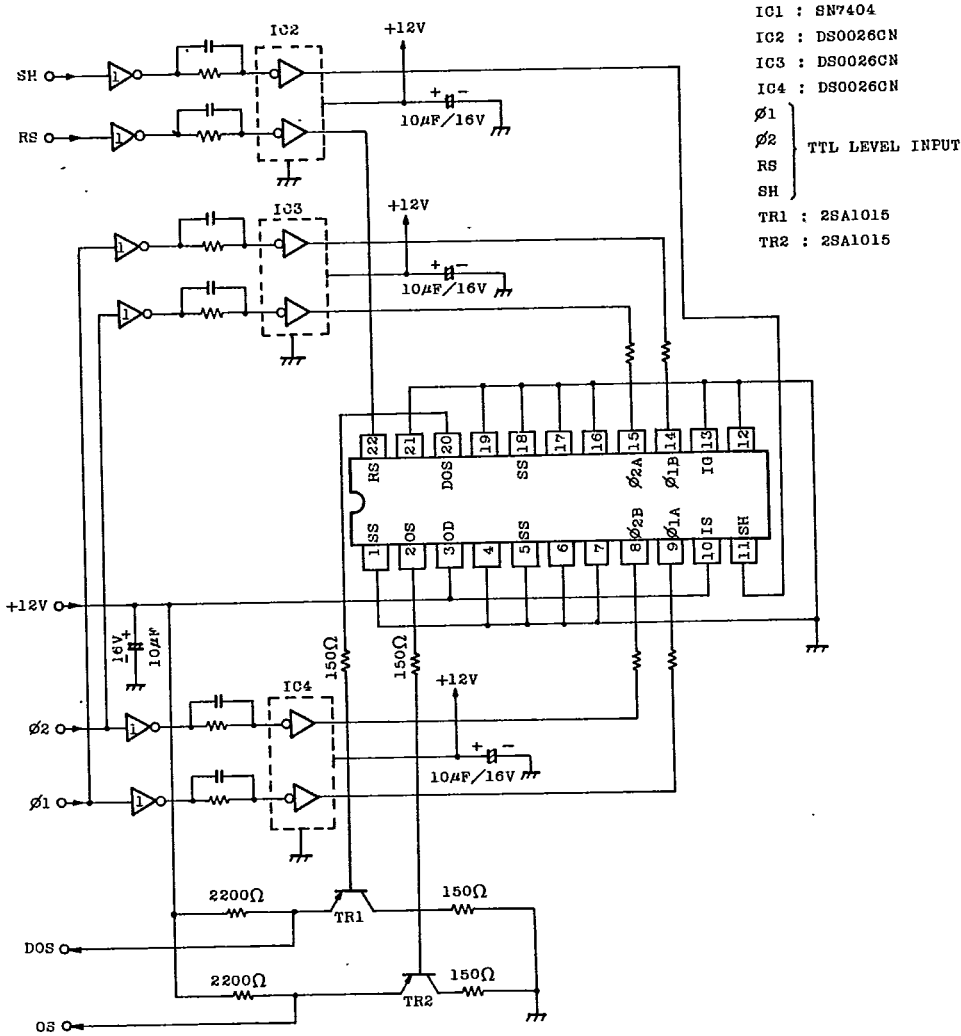
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TYPICAL DRIVE CIRCUITRY



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T-41-55

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CAUTION

1. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂ or Freon Gas.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

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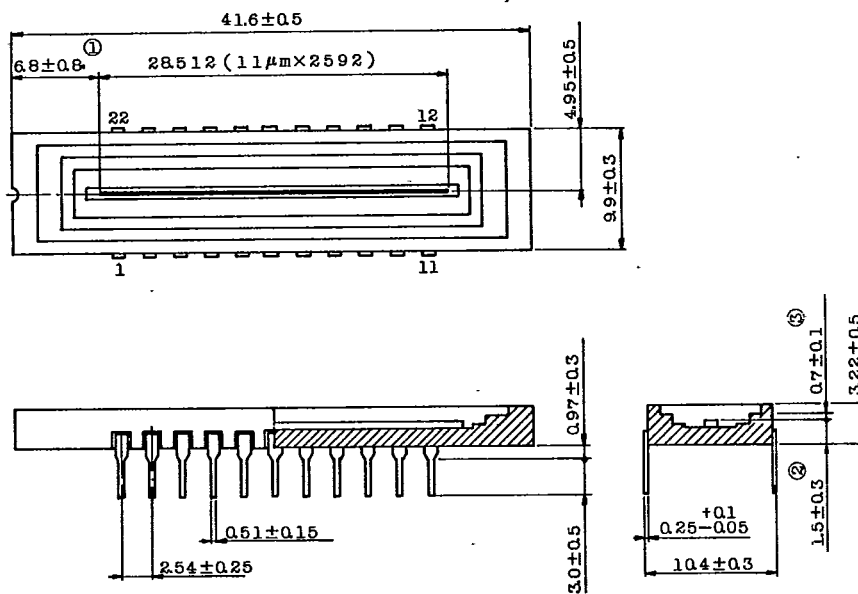
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T-41-55

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PACKAGE OUTLINE (4D22G-C)

Unit in mm



- ① No. 1 SENSOR ELEMENT(S1) TO EDGE OF PACKAGE.
- ② TOP OF CHIP TO BOTTOM OF CERAMIC.
- ③ GLASS THICKNESS (n=1.5)