

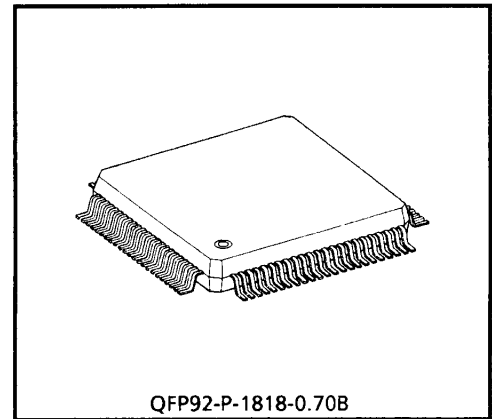
# T6A40

## ROW DRIVER FOR A DOT MATRIX LCD

The T6A40 is a 68-channel-output row driver for an STN dot matrix LCD. The T6A40 features -28-V LCD drive voltage. The T6A40 is able to drive LCD panels with a duty ratio of up to 1/240. It is recommended for use with the T6A39.

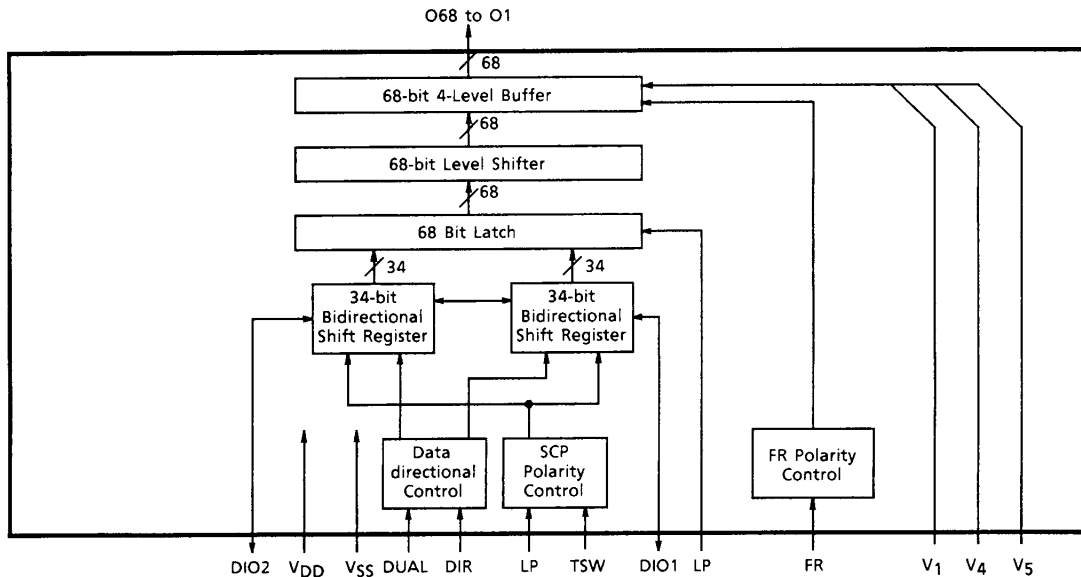
### FEATURES

- Display duty application : to 1/240
- LCD drive signal : 68
- Data transfer : 1-bit bidirectional
  - ① O68←O1
  - ② O68→O1
  - ③ O1→O34, O35←O68
- LCD drive voltage : -8 to -28V (max -30V)
- Operating voltage : 4.5 to 5.5V
- Operating temperature : -20 to 75°C
- LCD drive output resistance : 1.5kΩ (max) (12.8V, 1/9 bias)
- LCD drive output timing : Change on falling edge of LP



Weight : 1.45g (typ.)

### BLOCK DIAGRAM



961001EBA2

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## PIN FUNCTIONS

PIN NAME	I/O	FUNCTIONS	LEVEL
O1 to O68	Output	Output for LCD drive signal	$V_{DD}$ to $V_5$
DIO1, DIO2	I/O	Input/output for shift data	$V_{DD}$ to $V_{SS}$
LP	Input	(Shift Clock Pulse) Input for shift clock pulse	
FR	Input	(Frame) Input for frame signal	
DUAL	Input	(Dual Mode) Terminal for dual input mode or single input mode select	
DIR	Input	(Direction) Input for data flow direction select	
TSW	Input	(Terminal Switch) When tied to $V_{SS}$ : (O1 to O68) output on the rising edge of LP When tied to $V_{DD}$ : (O1 to O68) output on the falling edge of LP	
$V_{DD}$	—	Power supply for internal logic (5V)	—
$V_{SS}$	—	Power supply for internal logic (0V)	
$V_1$	—	Power supply for LCD drive circuit	
$V_4$	—	Power supply for LCD drive circuit	
$V_5$	—	Power supply for LCD drive circuit	

## RELATION BETWEEN FR, DATA INPUT AND OUTPUT LEVEL

FR	DATA INPUT (DIO1, DIO2)	OUTPUT LEVEL
L	L	$V_1$
L	H	$V_5$
H	L	$V_4$
H	H	$V_{DD}$

## DATA INPUT FORMAT

DUAL	DIR	DATA FLOW	DATA INPUT	
			DIO1	DIO2
$V_{DD}$	$V_{DD}$	O1→O34	IN	IN
		O68→O35		
$V_{SS}$	$V_{DD}$	O1→O68	IN	OUT
$V_{DD}$	$V_{SS}$	O68→O1	OUT	IN
$V_{SS}$	$V_{SS}$			



**ABSOLUTE MAXIMUM RATINGS**(Ensure that the following conditions are maintained,  $V_{DD} \geq V_1 \geq V_4 \geq V_5$ ,  $V_{SS} = 0V$ )

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	$V_{DD}$	$V_{DD}$	- 0.3 to 7.0	V
Supply Voltage 2	$V_1$	$V_1$	$V_{DD} - 30.0$ to $V_{DD} + 0.3$	V
Supply Voltage 3	$V_4$	$V_4$	$V_{DD} - 30.0$ to $V_{DD} + 0.3$	V
Supply Voltage 4	$V_5$	$V_5$	$V_{DD} - 30.0$ to $V_{DD} + 0.3$	V
Input Voltage	$V_{IN}$	(*1)	- 0.3 to $V_{DD} + 0.3$	V
Operating Temperature	$T_{opr}$	—	- 20 to 75	°C
Storage Temperature	$T_{stg}$	—	- 55 to 125	°C

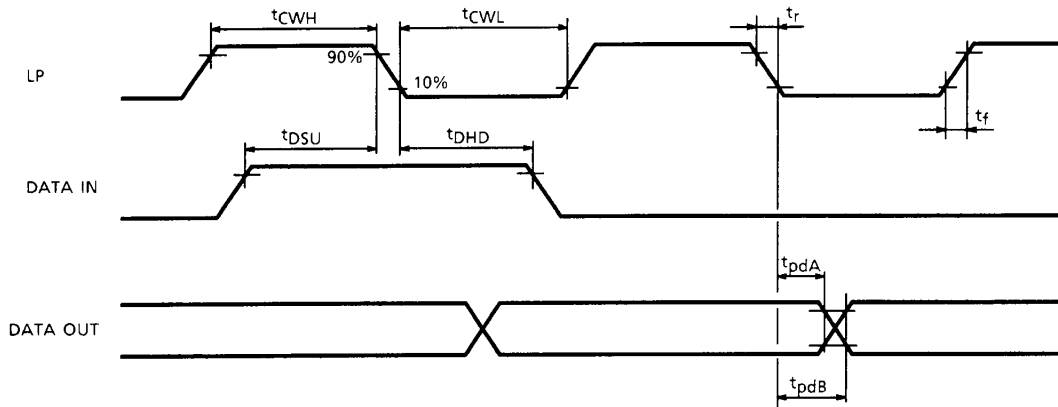
(\*1) FR, DIR, DIO1, DIO2, DUAL, TSW, LP

**ELECTRICAL CHARACTERISTICS****DC CHARACTERISTICS**TEST CONDITIONS (Unless otherwise noted,  $V_{SS} = 0V$ ,  $V_{DD} = 4.5V$  to  $5.5V$ ,  $V_5 = (V_{DD} - 23)V \pm 10\%$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	PIN NAME	
Supply Voltage 1	$V_{DD}$	—	—	4.5	5.0	5.5	V	$V_{DD}$	
Supply Voltage 2	$V_5$	—	—	$V_{DD} - 28$	—	$V_{DD} - 8.0$	V	$V_5$	
Input Voltage	H Level	$V_{IH}$	(*2)	$V_{DD} - 0.8$	—	$V_{DD}$	V	FR, DIR, DIO1, DIO2, DUAL, LP, TSW	
	L Level	$V_{IL}$	(*2)	0	—	0.8			
Output Voltage	H Level	$V_{OH}$	$I_{OH} = -0.5mA$	$V_{DD} - 0.5$	—	$V_{DD}$	V	DIO1, DIO2	
	L Level	$V_{OL}$	$I_{OL} = 0.5mA$	—	—	0.5			
Output Resistance	H Level	$R_{OH}$	$V_{OUT} = V_{DD} - 0.5V$ (*3)	—	—	1.2	k $\Omega$	O1 to O68	
	M Level	$R_{OM}$	$V_{OUT} = V_1 \pm 0.5V$ (*3)	—	—	1.2			
	M Level	$R_{OM}$	$V_{OUT} = V_4 \pm 0.5V$ (*3)	—	—	1.2			
	L Level	$R_{OL}$	$V_{OUT} = V_5 + 0.5V$ (*3)	—	—	1.2			
Current Consumption	$I_{SS}$	—	$V_{DD} = 5.5V$ $V_5 = -22.5V$ $f_{FR} = 35.5Hz$ $f_{LP} = 7.1kHz$ 01 to 068 : no load	Input Data : $f_{DIO} = 71Hz$ (Duty : 1/100) Input Voltage : H = $V_{DD}$ L = $V_{SS}$ (*3)	—	2.0	4.0	$\mu A$	$V_{SS}$

(\*2)  $R_L = 3k\Omega$ ,  $C_L = 1500pF$ (\*3)  $V_{DD} = 5.0V$ ,  $V_5 = -7.8V$ ,  $V_1 = V_{DD} - 1/9(V_{DD} - V_5)$ ,  $V_4 = V_{DD} - 8/9(V_{DD} - V_5)$

AC CHARACTERISTICS



TEST CONDITIONS ( $V_{SS} = 0V$ ,  $V_{DD} = 4.5$  to  $5.5V$ ,  $V_5 = (V_{DD} - 23)V \pm 10\%$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
SCP Pulse Width H	$t_{CWH}$	LP	30	—	ns
SCP Pulse Width L	$t_{CWL}$	LP	1	—	$\mu s$
Input Rise / Fall Time	$t_r, t_f$	LP, FR, DIO1, DIO2	—	50	ns
Data Set-up Time	$t_{DSU}$	DIO1, DIO2	30	—	ns
Data Hold Time	$t_{DHD}$	DIO1, DIO2	50	—	ns
Output Data Delay Time A (*4)	$t_{pdA}$	DIO1, DIO2	80	—	ns
Output Data Delay Time B (*4)	$t_{pdB}$	DIO1, DIO2	—	1	$\mu s$

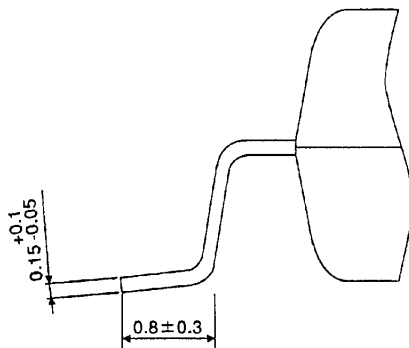
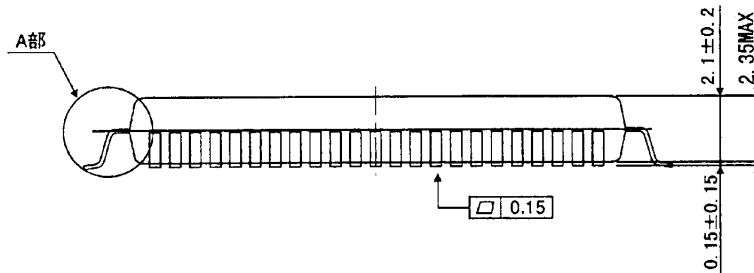
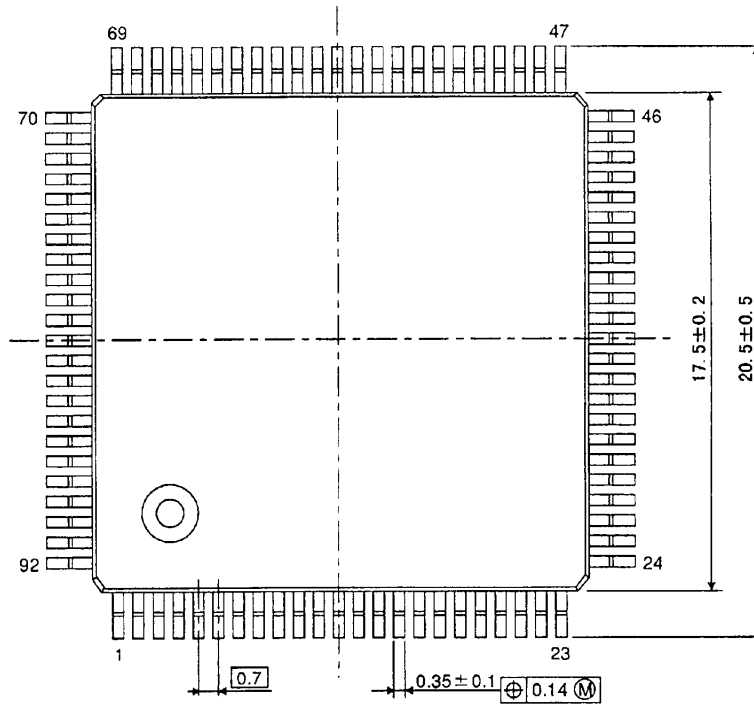
(\*4)  $C_L = 10pF$

NOTE

Insert the bypass capacitor ( $0.1\mu F$ ) between  $V_{DD}$  and  $V_{SS}$  to decrease power supply noise.  
Place the bypass capacitor as close to the LSI as possible.

OUTLINE DRAWING  
QFP92-P-1818-0.70B

Unit : mm



Weight : 1.45g (Typ.)