

OKI semiconductor

MSM5832RS

REAL TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

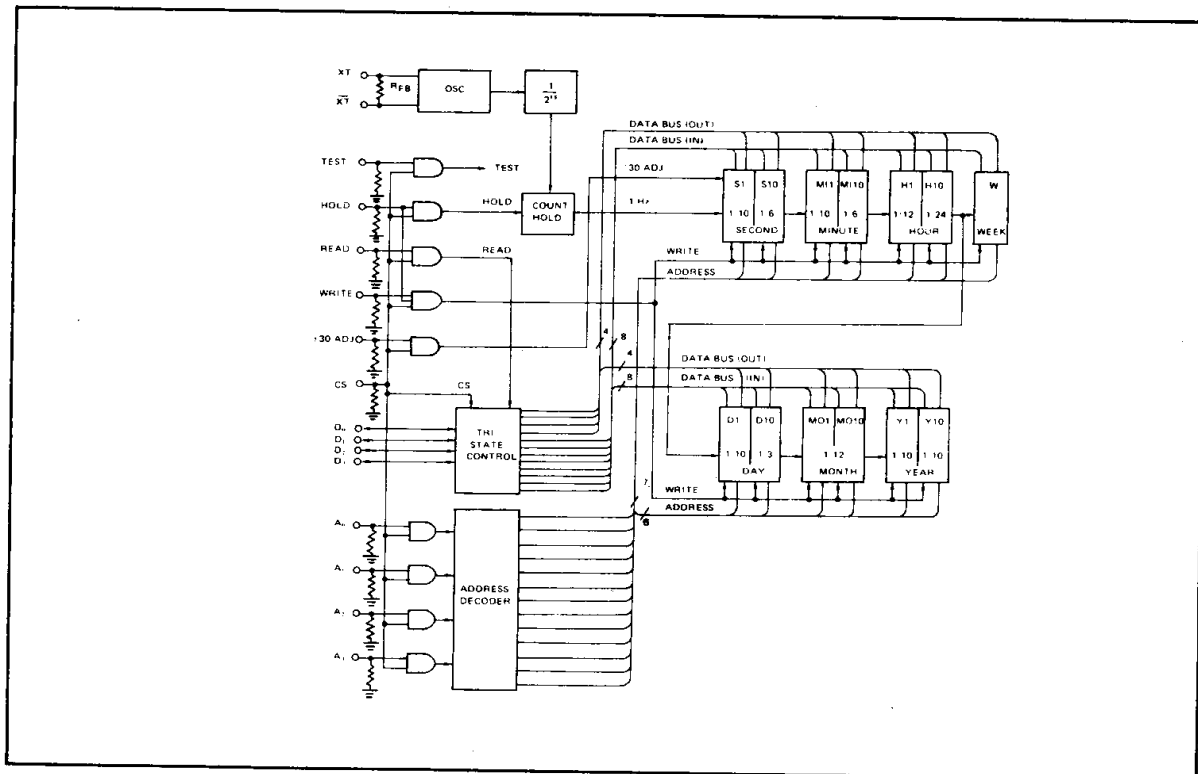
The MSM5832RS is a metal-gate CMOS Real Time Clock/Calendar for use in bus-oriented microprocessor applications. The on-chip 32.768kHz crystal controlled oscillator time base is divided to provide addressable 4-bit I/O data of SECONDS, MINUTES, HOURS, DAY-OF-WEEK, DATE, MONTH, and YEAR. Data access is controlled by 4-bit address, chip select, read, write and hold inputs. Other functions include 12H/24H format selection, leap year identification and manual ± 30 second correction.

The MSM5832RS normally operates from a 5V $\pm 5\%$ supply. Battery backup operation down to 2.2V allows continuation of time keeping when main power is off. The MSM5832RS is offered in an 18-lead dual-in-line plastic (RS suffix) package.

FEATURES

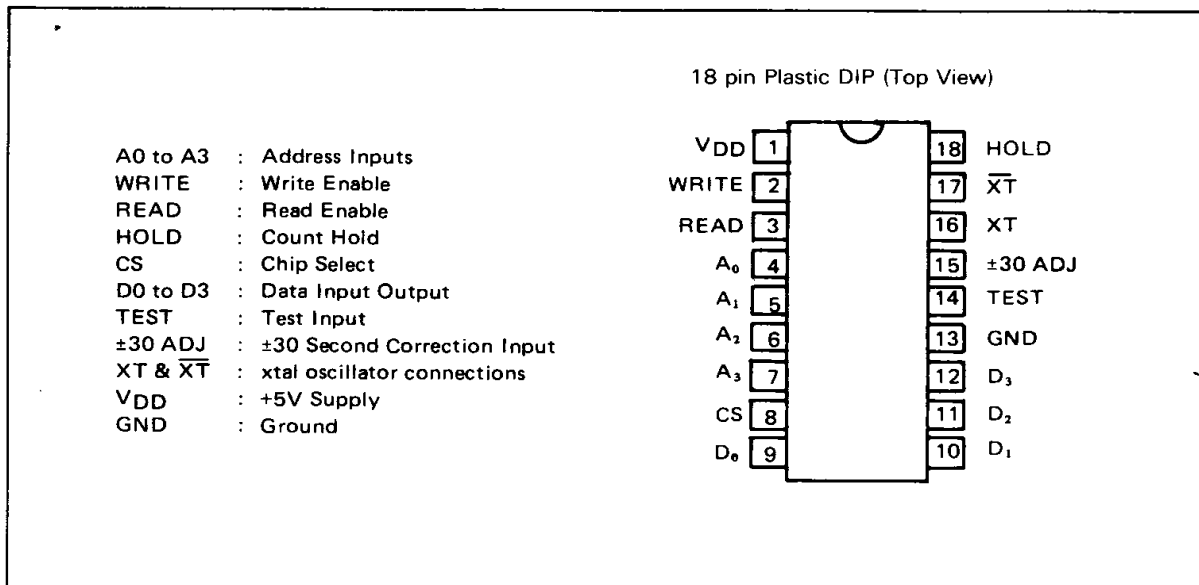
- 7 Function – SECOND, MINUTE, HOUR, DAY, DAY-OF-WEEK, MONTH, YEAR
- Automatic leap year calendar
- 12 or 24 hour format
- ± 30 second error correction
- 4-BIT DATA BUS
- 4-BIT ADDRESS
- READ, WRITE, HOLD, and CHIP SELECT inputs
- Reference signal outputs – 1024, 1, 1/60, 1/3600Hz
- 32.768kHz crystal controlled operation
- Single 5V power supply
- Back-up battery operation to $V_{DD} = 2.2V$
- Low power dissipation
 - 90 μW Max. at $V_{DD} = 3V$
 - 2.5 mW Max. at $V_{DD} = 5V$
- 18 pin plastic DIP (DIP18-P-300)

FUNCTIONAL BLOCK DIAGRAM



5

PIN CONFIGURATION



REGISTER TABLE

Address Input				Register Name	Data Input/Output				Data Limit	Remarks
A ₀	A ₁	A ₂	A ₃		D ₀	D ₁	D ₂	D ₃		
0	0	0	0	S1	*	*	*	*	0 ~ 9	S1 or S10 are reset to zero irrespective of input data D0–D3 when write instruction is executed with address selection.
1	0	0	0	S10	*	*	*		0 ~ 5	
0	1	0	0	M11	*	*	*	*	0 ~ 9	
1	1	0	0	M110	*	*	*		0 ~ 5	
0	0	1	0	H1	*	*	*	*	0 ~ 9	D2 = "1" for PM D3 = "1" for 24 hour format D2 = "0" for AM D3 = "0" for 12 hour format
1	0	1	0	H10	*	*	†	†	0 ~ 1 0 ~ 2	
0	1	1	0	W	*	*	*		0 ~ 6	
1	1	1	0	D1	*	*	*	*	0 ~ 9	
0	0	0	1	D10	*	*	†		0 ~ 3	D2 = "1" for 29 days in month 2 (2) D2 = "0" for 28 days in month 2
1	0	0	1	MO1	*	*	*	*	0 ~ 9	
0	1	0	1	MO10	*				0 ~ 1	
1	1	0	1	Y1	*	*	*	*	0 ~ 9	
0	0	1	1	Y10	*	*	*	*	0 ~ 9	

(1) *data valid as "0" or "1".

Blank does not exist (unrecognized during a write and held at "0" during a read)

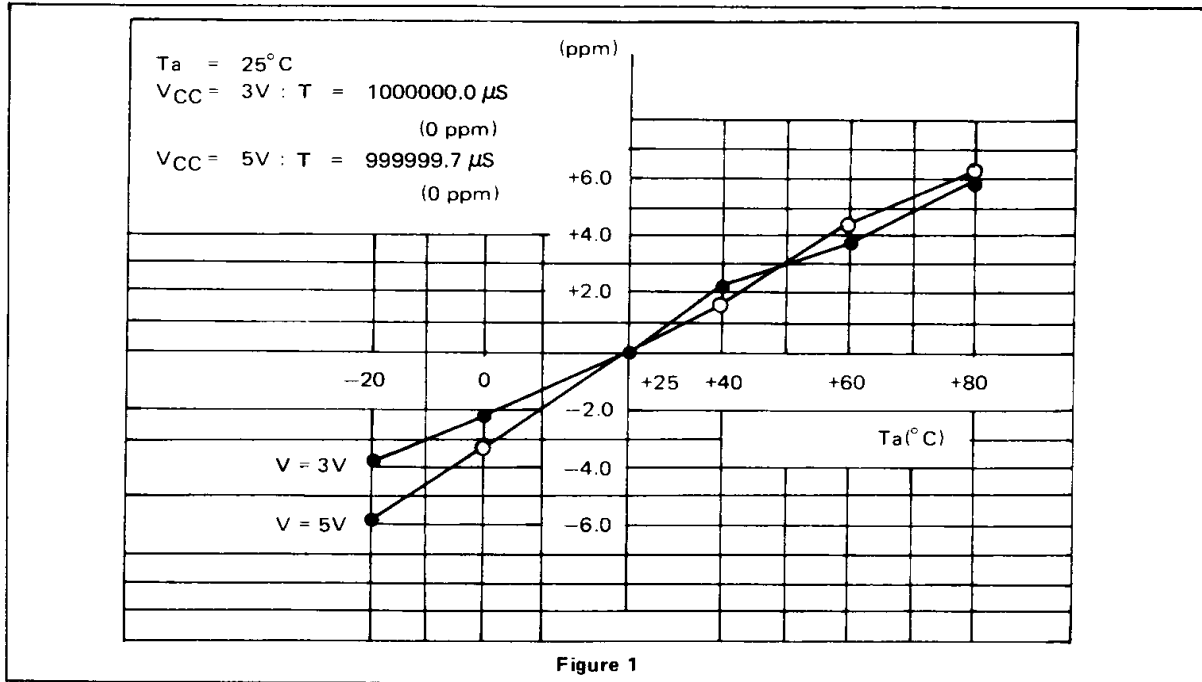
†data bits used for AM/PM, 12/24 HOUR and leap year.

(2) If D2 previously set to "1", upon completion of month 2 day 29, D2 will be internally reset to "0".

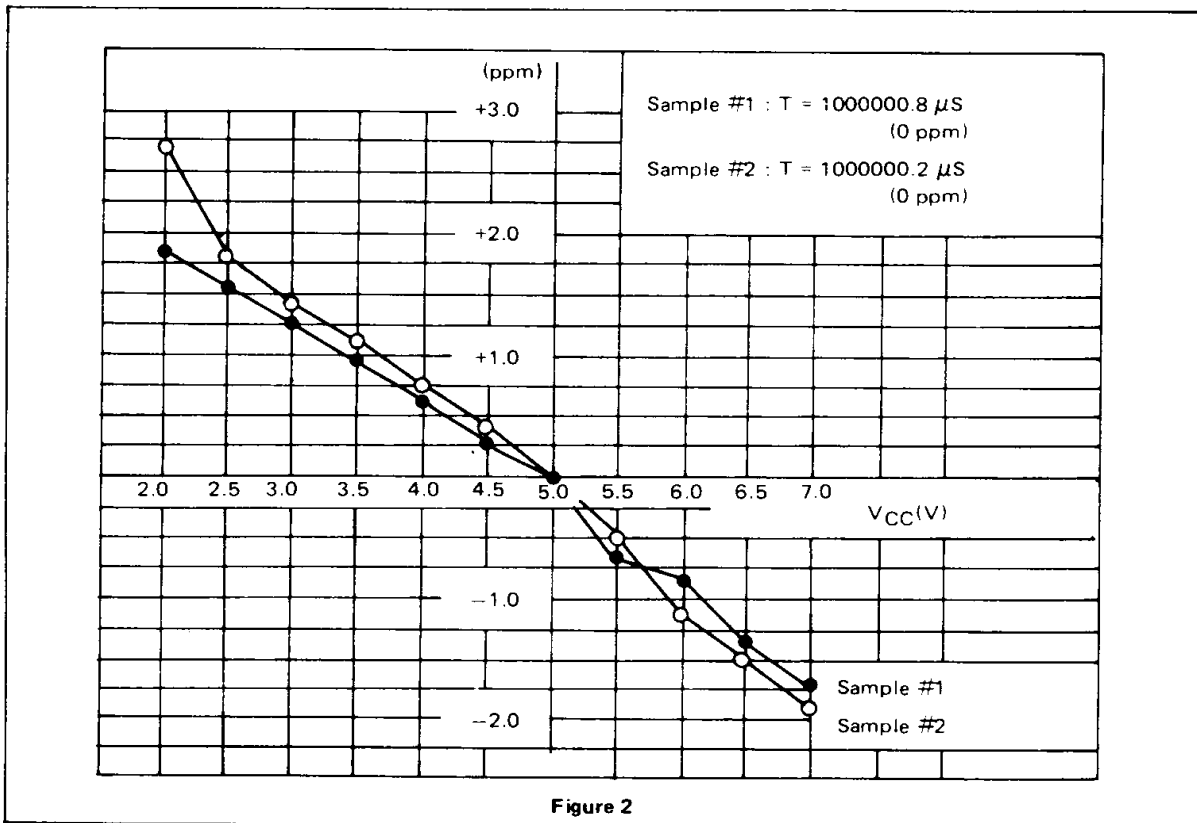
Table 1

OSCILLATOR FREQUENCY DEVIATIONS

Frequency Deviation vs Temperature



Frequency Deviation vs Supply Voltage



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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V _{DD}	-0.3 ~ 7.0	V
Input voltage	V _I	-0.3 ~ V _{DD} + 0.3	V
Data I/O voltage	V _O	-0.3 ~ V _{DD} + 0.3	V
Storage Temperature	T _{stg}	-55 ~ 150	°C

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V _{DD}	4.5	5	7	V	
Standby Supply Voltage	V _{DH}	2.2	-	7	V	
Input Signal Level	V _{IH}	3.6	-	V _{DD}	V	V _{DD} = 5V ± 5% Respect to GND
	V _{IL}	-0.3	-	0.8	V	
Crystal Oscillator Freq.	f(XT)	-	32.768	-	kHz	
Operating Temperature	T _{OP}	-30	-	+85	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ± 5%; T_A = -30 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Current (1)	I _{IH}	10	25	50	μA	V _{IN} =5V, V _{DD} =5V
	I _{IL}	-	-	-1	μA	V _{IN} = 0V
Data I/O Leakage Current	I _{LD}	-10	-	10	μA	V _{I/O} = 0 to V _{DD} CS = "0"
Output Low Voltage	V _{OL}	-	-	0.4	V	I _O = 1.6 mA, CS = "1", READ = "1"
Output Low Current	I _{OL}	1.6	-	-	mA	V _O = 0.4V, CS = "1", READ = "1"
Operating Supply Current	I _{DDS}	-	15	30	μA	V _{CC} = 3V, T _a = 25°C
	I _{DD}	-	100	500	μA	V _{CC} = 5V, T _a = 25°C

(1) XT, XT̄ and D₀ ~ D₃ excluded.

SWITCHING CHARACTERISTICS

(1) READ mode

($V_{DD} = 5V \pm 5\%$, $T_a = 25^\circ C$)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
HOLD Set-up Time	t_{HS}	-----	150	—	—	μs
HOLD Hold Time	t_{HH}	-----	0	—	—	μs
HOLD Pulse Width	t_{HW}	-----	—	—	990	ms
HOLD "L" Hold Time	t_{HL}	-----	130	—	—	μs
READ Hold Time	t_{RH}	-----	0	—	—	μs
READ Set-up Time	t_{RS}	-----	0	—	—	μs
READ Access Time	t_{RA}	$R_{PULL-UP} = 5K\Omega$ $C_L = 15pF$	—	—	6	μs
ADDRESS Set-up Time	t_{AS}	-----	3	—	—	μs
ADDRESS Hold Time	t_{AH}	-----	0.2	—	—	μs
READ Pulse Width	t_{RW}	$R_{PULL-UP} = 5K\Omega$ $C_L = 15pF$	2	—	—	μs
DARA Access Time	t_{AC}	$R_{PULL-UP} = 5K\Omega$ $C_L = 15pF$	—	—	0.6	μs
OUTPUT Disable Time	t_{OFF}	$R_{PULL-UP} = 5K\Omega$ $C_L = 15 pF$	—	—	0.6	μs
CS Enable Delay Time	t_{CS1}	-----	—	—	0.6	μs
CS Disable Delay Time	t_{CS2}	-----	—	—	0.6	μs

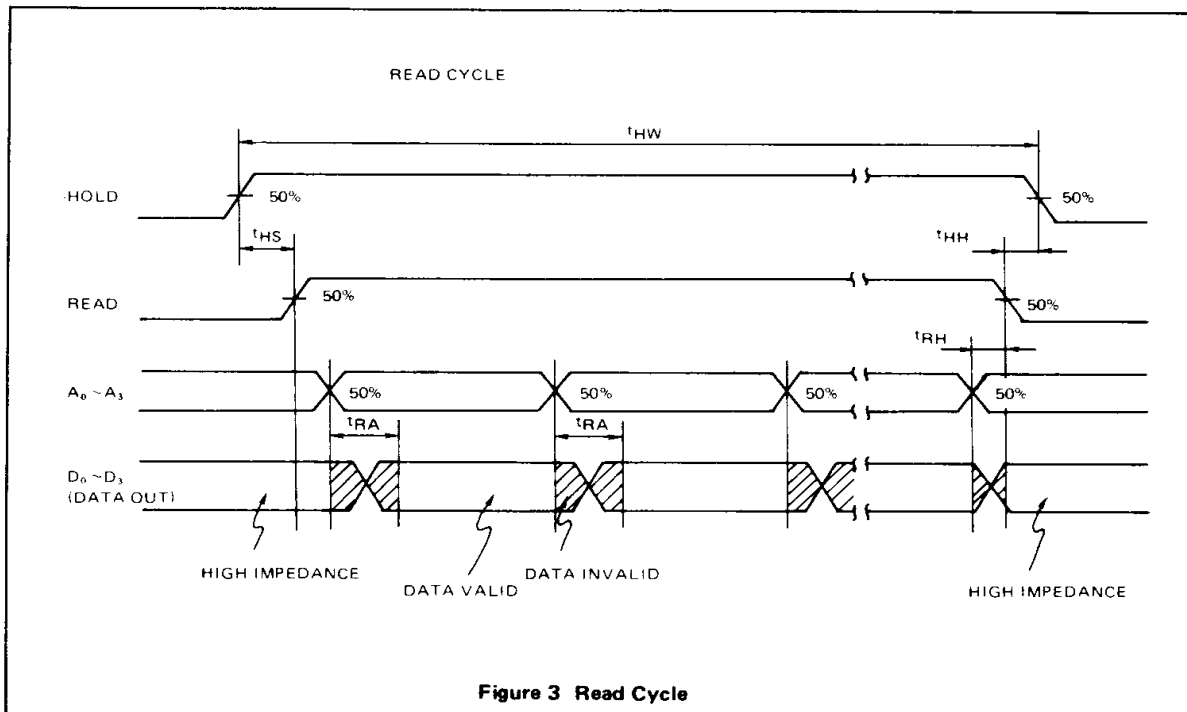


Figure 3 Read Cycle

- Notes: 1. A Read occurs during the overlap of a high CS and a high READ.
 2. CS may be a permanent "1", or may be coincident with HOLD pulse.

SWITCHING CHARACTERISTICS

(2) WRITE mode

($V_{DD} = 5V \pm 5\%$, $T_a = 25^\circ C$)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
HOLD Set-up Time	t_{HS}	——	150	—	—	μs
HOLD Hold Time	t_{HH}	——	0	—	—	μs
HOLD Pulse Width	t_{HW}	——	—	—	990	ms
HOLD "L" Hold Time	t_{HL}	——	130	—	—	μs
ADDRESS Pulse Width	t_{AW}	——	1.7	—	—	μs
Data Pulse Width	t_{DW}	——	1.7	—	—	μs
DATA Set-up Time	t_{DS}	——	0.5	—	—	μs
DATA Hold Time	t_{DH}	——	0.2	—	—	μs
WRITE Pulse Width	t_{WW}	——	1.0	—	—	μs
CS Enable Delay Time	t_{CS1}	——	—	—	0.6	μs
CS Disoble Delay Time	t_{CS2}	——	—	—	0.6	μs

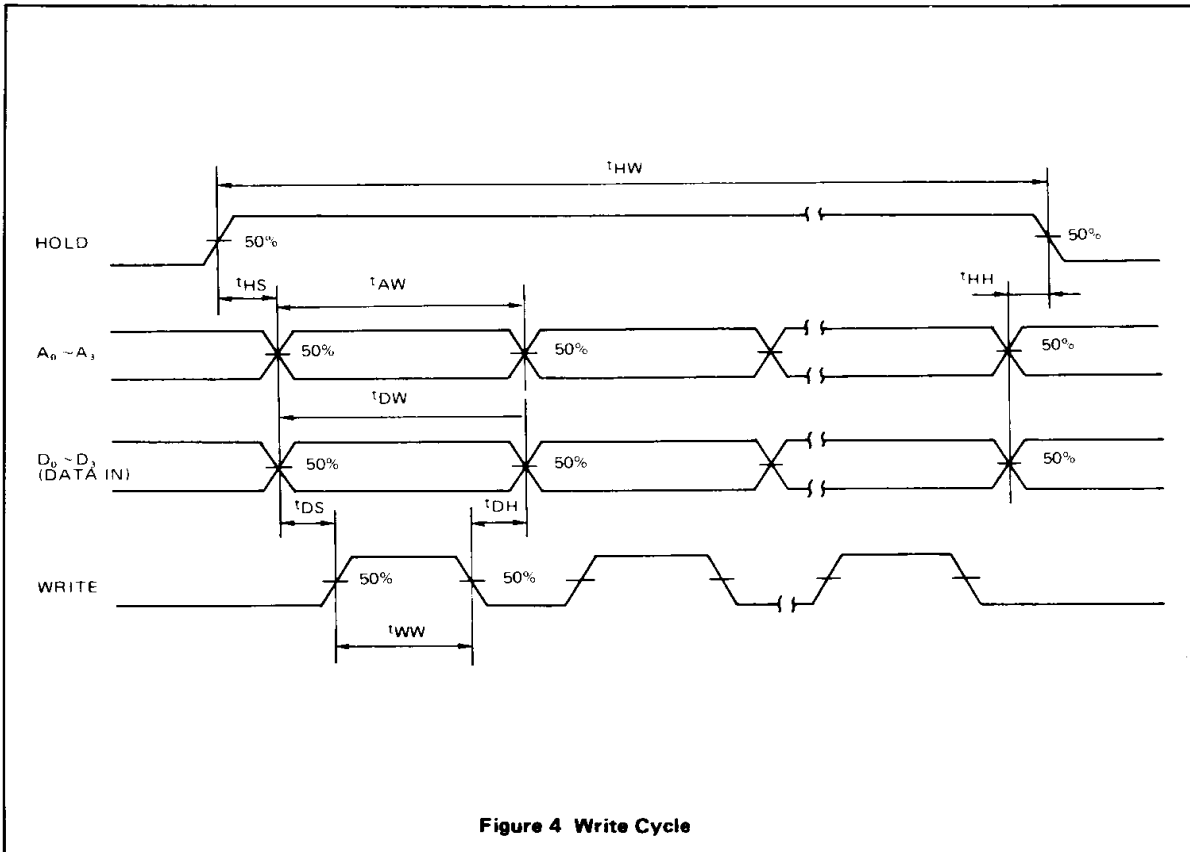
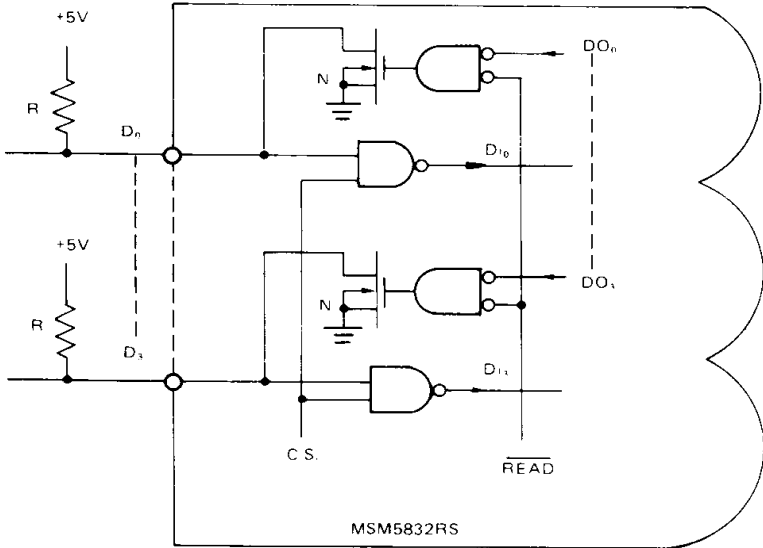


Figure 4 Write Cycle

- Notes:** 1. A WRITE occurs during the overlap of a high CS, a high HOLD and a high WRITE.
 2. CS may be permanent "1", or may be coincident with HOLD pulse.

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PIN DESCRIPTION

Name	Pin No.	Description
VDD	1	Power supply pin. Application circuits for power supply are described in Figure 9.
WRITE	2	Data write pin. Data write cycle is described in Figure 4.
READ	3	Data read pin. Data read cycle is described in Figure 3.
A ₀ ~ A ₃	4 ~ 7	Address input pins used to select internal counters for read/write operations. The address is specified by 4-bit binary code as shown in Table 1.
C S	8	Chip select pin which is required to interface with the external circuit. HOLD, WRITE, READ, ±30ADJ, TEST, D ₀ ~ D ₃ and A ₀ ~ A ₃ pins are activated if CS is set at H level, while all of these pins are disabled if CS is set at L level.
D ₀ ~ D ₃	9 ~ 12	<p>Data input/output pins (bidirectional bus). As shown in Figure 5, external pull-up registers of 4.7 kΩ ~ 10 kΩ are required by the open-drain NMOS output. D₃ is the MSB, while D₀ is the LSB</p> 

5

Figure 5

■ PERIPHERALS · MSM5832RS ■

Name	Pin No.	Description
GND _s	13	Ground pin.
TEST	14	Test pin. Normally this pin should be left open or should be set at ground level. With CS at V_{DD} , pulses to V_{DD} on the TEST input will directly clock the S_1 , $M1_{10}$, W , D_1 and Y_1 counters, depending on which counter is addressed (W and D_1 are selected by D_1 address in this mode only). Roll-over to next counter is enabled in this mode.
± 30 ADJ	15	This pin is used to adjust the time within the extent of ± 30 seconds. If this pin is set at H level when the seconds digits are 0 ~ 29, the seconds digits are cleared to 0. If this pin is set at H level when the seconds digits are 30 ~ 59, the second digits will be cleared to 0 and the minutes digits will be increased by +1. To enable this function, 31.25 ms or more width's pulse should be input to this pin.
XT	16	<p>Oscillator pin. 32.768 kHz crystal, capacitor and trimmer condenser for frequency adjustment connected to these pins. See Figure 6. As for oscillator frequency deviation, refer to Figure 1 and Figure 2.</p> <p>If an external clock is to be used for the MSM5832RS's oscillation source, the external clock is to be input to XT, and \overline{XT} should be left open.</p>
\overline{XT}	17	
<p>Figure 6</p>		
HOLD	18	Switching this input to V_{DD} inhibits the internal 1 Hz clock to the S_1 counter. After the specified HOLD set-up time (150 μ s), all counters will be in a static state, thus allowing error-free read or write operations. So long as the HOLD pulse width is less than 990 ms, real time accuracy will be undisturbed. Pull-down to GND is provided by an internal resistor.

REFERENCE SIGNAL OUTPUT PIN

Condition	Output	Reference Frequency	Pulse Width
HOLD = L	D ₀ ⁽¹⁾	1024 Hz	duty 50%
READ = H	D ₁	1 Hz	122.1 μs
CS = H	D ₂	1/60 Hz	122.1 μs
A ₀ ~ A ₃ = H	D ₃	1/3600 Hz	122.1 μs

(1) 1024 Hz signal at D₀ not dependent on HOLD input level.

APPLICATION EXAMPLE

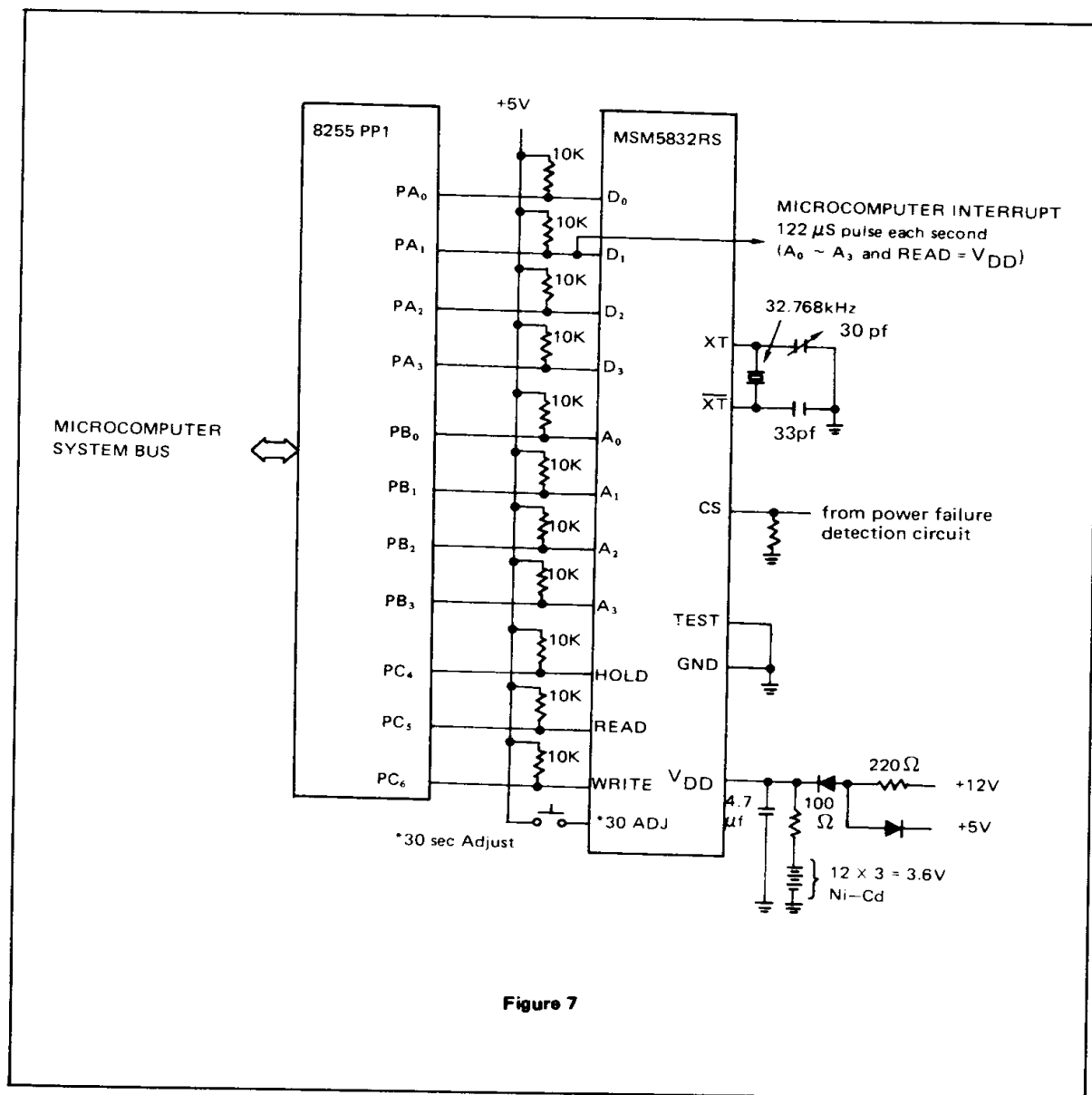
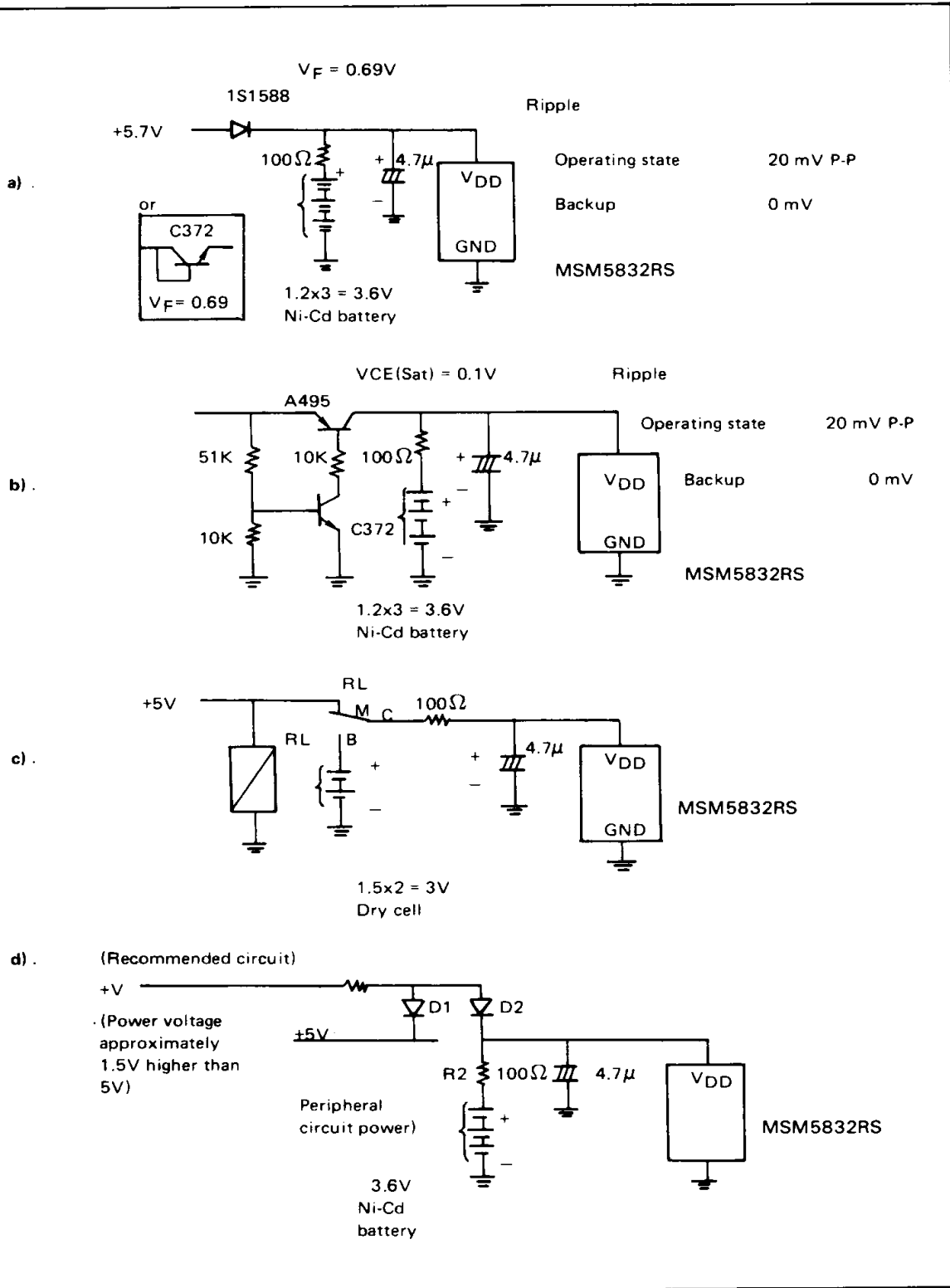


Figure 7

APPLICATION CIRCUIT — POWER SUPPLY CIRCUIT

Open or ground unused pins (pins other than the XT, XT̄, D0–D3, and BUSY pins).



Note: Use the same diodes for D1 and D2 to reduce the level difference between +5V and V_{DD} of the MSM5832RS.

5