APPLYING MODERN CLOCK DRIVERS TO MOS MEMORIES

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input wave forms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAM's (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, two new monolithic integrated circuit drivers, the MH0025 and MH0026 are selected as examples because of their low cost.

The MH0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage-gold doped process utilizing a collector sinker to minimize $V_{CE\,SAT}$.

The MH0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Of course each of us is careful of details but reminders such as "turn on the power supplies" or "don't reverse supply polarity" sometimes solve a not-so-obvious problem. This section is intended to review and answer design questions like "how much should I decouple supplies?"

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking

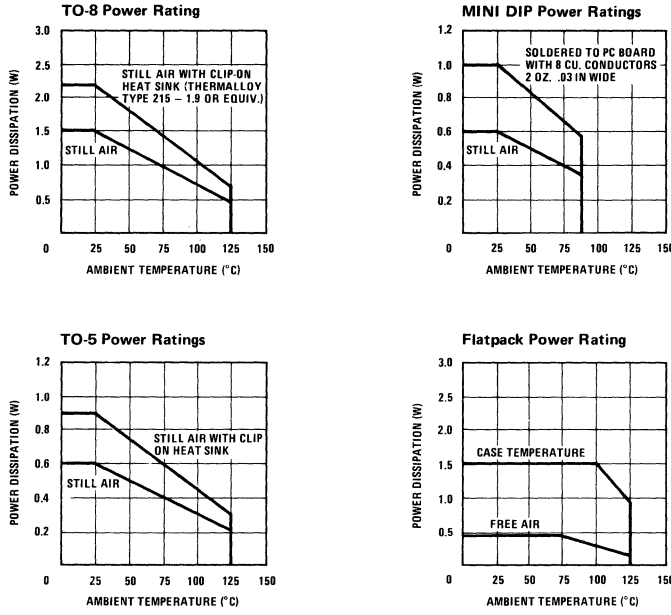
TABLE I. MH0025 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0.0022μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0.0001μF, R_O = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	$I_{IN} \triangleq$ 10mA, I_{OUT} = 1mA	$V^- + 1.0$	V
On Supply Current (V^+)	I_{IN} = 10mA	17	mA

TABLE II. MH0026 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		7.5	ns
t_{OFF}	C_{IN} = 0.001μF, R_{IN} = 0Ω	7.5	ns
t_r	R_0 = 50Ω, C_L = 1000pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = -1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 0.5$	V
On Supply Current (V^+)	I_{IN} = 10mA	28	mA

TABLE III. Package Power Ratings



required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

The TO-5 ("H") package is rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 900mW with clip on heat sink (derate at 6.0mW/°C above 25°C). This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on-heat sink increases driving capability by 50%.

The 8 pin ("N") molded mini-DIP is rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 1.0W soldered to P.C. board (derate at 6.6mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600mW when mounted in a socket and not one watt until it is soldered down.)

The TO-8 ("G") package is rated at 1.5W still air (derate at 10mW/°C above 25°C) and 2.3W with with clip on heat sink (Wakefield type 215-1.9 or equivalent-derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

The 14 pin cavity DIP is rated at 600mW free air. While some rate this package at 1W *case* temperature, National does not recommend its use for clock drivers. This is because from a user point of view, it is impossible to get more than 400 to 500mW rating under normal system conditions; i.e., there is no practical way to conduct heat away from the device other than air.

Other package types range in size and power handling capability. Most have the disadvantage of being in non-standard sizes and are difficult to mount in a system.

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

- Package and heat sink selection
- Average DC power, P_{DC}
- Average AC power, P_{AC}
- Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of DC power and AC power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \qquad (1)$$

Average DC power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \quad (2)$$

For most types of clock drivers, the first two terms are neglible (less than 10mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

Req = Equivalent device resistance in the "ON" state

$= V^+ - V^-/I_{S(ON)} \quad (3)$

DC = Duty Cycle

$= \frac{\text{"ON" Time}}{\text{"ON" Time + "OFF" Time}}$

For the MH0025, Req is typically 1kΩ while Req is typically 600Ω for the MH0026. Graphical solutions for P_{DC} appear in Figure 1. For example if $V^+ = +5V$, $V^- = -12V$, Req = 500Ω, and DC = 25%, then P_{DC} = 145mW. However, if the duty cycle was only 5%, P_{DC} = 29mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

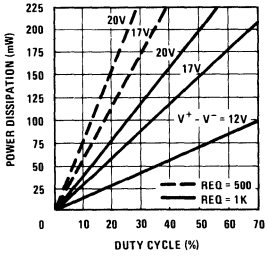


FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \quad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in Figure 2. Thus, any type of clock driver will dissipate internally 290mW per MHz per thousand pF of load. At 5MHz, this would be 1.5W for a 1000pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

Combining equations (1), (2), (3), and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

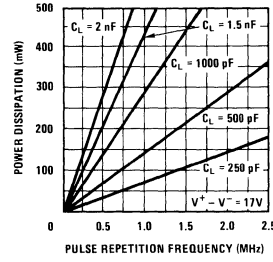


FIGURE 2. P_{AC} vs PRF

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \quad (5)$$

As an example, the MH0025CN can dissipate 630mW at $T_A = 70°C$ when soldered to a printed circuit board. Req is approximately equal to 1k. For $V^+ = 5V$, $V^- = -12V$, f = 1MHz, and DC = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(630 \times 10^{-3})}{(2)(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$$C_L \leq 880pF \text{ (each driver)}$$

A typical application might involve driving an MM5013 triple 64-bit shift register with the MH0025. Using the conditions above and the clock line capacitance of the MM5013 of 60pF, a single MH0025 can drive 880pF/60pF, or 14 MM5013's.

Similarly, the MH0026CG can dissipate 1.0W at 75°C. For $V^+ = 5V$, $V^- = -12V$, f = 2MHz, and DC = 20%, the maximum load capacitance which may be driven is:

$$C_L \leq 2 \times \frac{1}{10^6}\left[\frac{(1.0)}{(2)(17)^2} - \frac{0.2}{600}\right]$$

$$C_L \leq 700pF \text{ (each driver)}$$

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TABLE IV. Worst Case Maximum Drive Capability for MH0026*

PACKAGE TYPE		TO-8 WITH HEAT SINK		TO-8 FREE AIR		MINI-DIP SOLDERED DOWN		TO-5 AND MINI-DIP FREE AIR	
Max. Operating Frequency	Max. Ambient Temp. → / Duty Cycle ↓	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C
100kHz	5%	30 k	24 k	19 k	15 k	13 k	10k	7.5k	5.8k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2.7k	2k	1.5k	1.1k
1MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	430
2MHz	25%	1.4k	1.1k	850	650	550	400	280	190
5MHz	25%	620	470	380	290	240	170	120	80
10MHz	25%	280	220	170	130	110	79	–	–

*Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$. For loads greater than 1200 pF, rise and fall times will be limited by output current.

Returning to the MM5013 example, a single MH0026 can drive 700pF/60pF, or 11 5013's. Using the above equations, Table IV has been calculated for quick reference. In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, AC power (which depends on frequency, voltage across the device, and capacitive load) and DC power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (c) peak transient current available. Details of these are included in Appendixes I and II. Figures AI-3, AI-4, AII-2, and AIII-3 illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver, and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ peak}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this app. note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vise versa for fall times. Since MOS logic is inverted from normal TTL, "risetime" as used in this note is "voltage fall" and "fall time" is "voltage rise."

Power Supply Decoupling

Although power supply decoupling is a wide spread and accepted practice, the question often arises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in Figure 3. In this instance, a small damping resistor is inserted

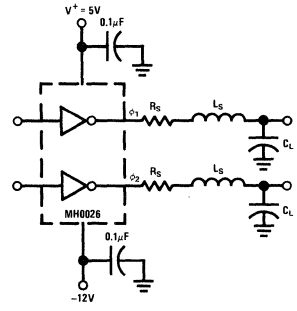

FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r\,(max)} = t_{f\,(max)} \leq 2.2\ R_S\ C_L \qquad (7)$$

One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2 f C_L$ and accordingly the resistor wattage rating will generally be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. Figure 4

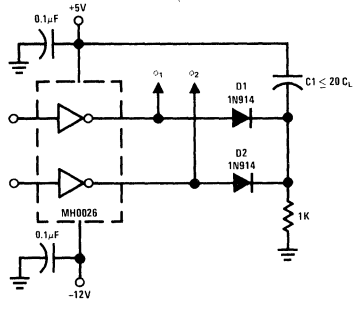

FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice versa) during the transition of ϕ_1 to MOS logic "1." The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Figure 5 illustrates the problem.

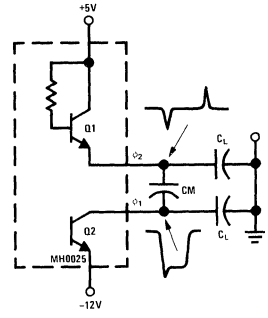

FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q_1 is "OFF" since only μA are drawn from the device. A simple method of minimizing cross-talk is shown in Figure 6.

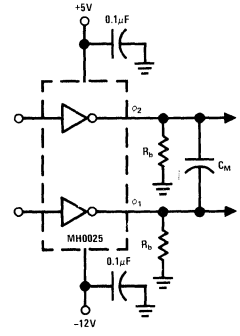

FIGURE 6. Use of Bleed Resistors to Minimize Clock-Line Crosstalk

Bleed resistors are connected between the clock driver and ground causing a current of a few mA to flow. The output impedance of the clock driver is reduced and the negative spike is thus minimized. Values for R_b depend on layout and the number of registers being driven. Typical values are between 1k and 10kΩ.

A major point should be emphasized with regard to clock-line crosstalk, i.e., even if the output impedance of the driver is zero ohms, self inductance between the clock driver and registers will cause the clock lines to spike on the transitions. Hence, the technique shown in Figure 6 works reasonably well for small systems.

For large systems, the circuit of Figure 7 is recommended. In this instance, Q_1 and Q_2 are turned "ON" just prior to the clocks transition to logic "1." The spike is therefore clamped by the $V_{CE\ (sat)}$ of Q_1 and Q_2. A key feature of the circuit is that the clamps are physically placed adjacent the register thus minimizing the inductance between the clamp and the load.

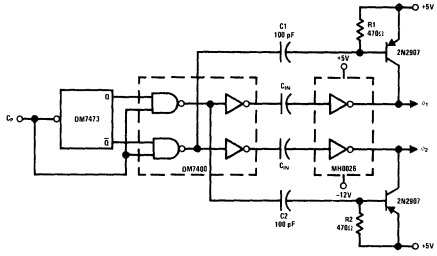

FIGURE 7. Cross Talk Minimization Circuit

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to DC level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the MH0025 and MH0026 utilize input capacitors when level shifting from TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of both the MH0025 and MH0026.

CONCLUSION

The practical aspects of driving MOS memories with new low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the MH0025 and MH0026 provide superior performance for most MOS input interface applications.

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1. Bert Mitchell, *"New MOS Clock Driver for MOS Shift Registers,"* National Semiconductor, AN-18, March 1969.

2. John Vennard, *"MOS Clock Drivers,"* National Semiconductor, MB-9, December 1969.

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6. Richard Percival, *"Dynamic MOS Shift Registers can also simulate Stack and Silo Memories,"* Electronics Magazine, Nov. 8, 1971.

7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, Aug. 1971.

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APPENDIX I

MH0025 Circuit Operation

The schematic diagram of the MH0025 is shown in Figure AI-1. With the TTL driver in the logic "0" state Q_1 is "OFF" and Q_2 is "ON" and the output is at approximately one V_{BE} below the V^+ supply.

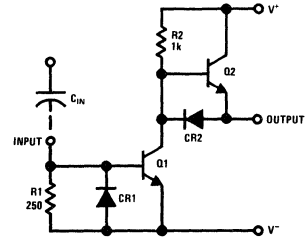

FIGURE AI-1. MH0026 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q_1, through C_{IN}, turning it "ON." As the collector of Q_1 goes negative, Q_2 turns OFF. Diode CR_2 assures turn-on of Q_1 prior to Q_2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q_2's base emitter junction.

The negative voltage transition (to MOS logic "1") will be quite linear since the capacitive load will force Q_1 into its linear region until the load is discharged and Q_1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q_1 turns "OFF" and Q_2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the MH0025 is primarily a function of the AC load, C_L, the available input current and total voltage swing. As shown in Figure AI-2, the input current must

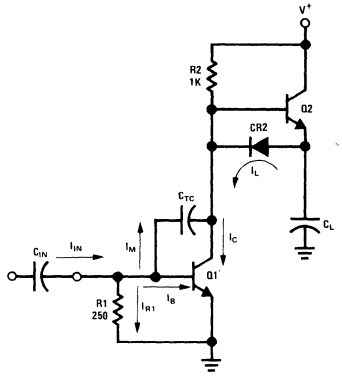

FIGURE AI-2. Rise Time Model for the MH0025

charge the Miller capacitance of Q_1, C_{TC}, as well as supply sufficient base drive to Q_1 to discharge C_L rapidly. By inspection:

$$I_{IN} = I_M + I_B + I_{R1} \qquad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M >> I_{R1} \text{ \& } I_B >> I_{R1}$$

$$I_B = I_{IN} - C_{TC}\frac{\Delta V}{\Delta t} \qquad \text{(AI-2)}$$

If the current through R_2 is ignored,

$$I_C = I_B h_{FEQ1} = I_L + I_M \qquad \text{(AI-3)}$$

where:

$$I_L = C_L \frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, AI-3 yields:

$$\frac{\Delta V}{\Delta t}[C_L + C_{TC}(h_{FEQ1}+1)] = h_{FEQ1} I_{IN} \qquad \text{(AI-4)}$$

or

$$t_r \cong \frac{[C_L + (h_{FEQ1}+1)C_{TC}]\,\Delta V}{h_{FEQ1} I_{IN}} \qquad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a MH0025 loaded with 1000 pF, rise times of:

$$\frac{(1000\text{pF} + 250\text{pF})\ (17\text{V})}{(50\text{mA})\ (20)}$$

or 21ns may be expected for V^+=5.0V, V^-=-12V. Figure AI-3 gives rise time for various values of C_L.

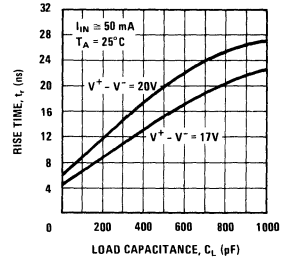

FIGURE AI-3. Rise Time vs C_L for the MH0025

Fall Time Considerations

The MOS logic fall time (voltage rise) of the MH0025 is dictated by the load, C_L, and the output capacitance of Q_1. The fall time equivalent circuit of MH0025 may be approximated with the circuit of Figure AI-4. In actual practice, the base

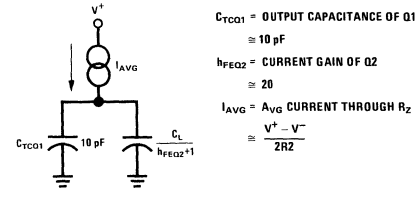

FIGURE AI-4. Fall Time Equivalent Circuit

drive to Q_2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic

values at the end. Figure AI-5 shows t_f as function of C_L.

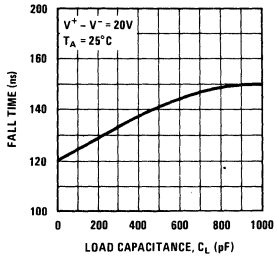

FIGURE AI-5. MH0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R_2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \qquad \text{(AI-6)}$$

or

$$t_f \cong 2R_2 \left(C_{TCQ1} + \frac{C_L}{h_{FEQ1+1}}\right) \qquad \text{(AI-7)}$$

MH0025 Input Drive Requirements

Since the MH0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50 to 60 mA region. It is therefore a good idea to drive the MH0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the MH0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The MH0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output

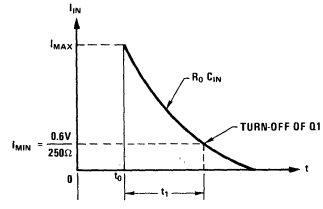

FIGURE AI-6. MH0025 Input Current Waveform

pulse width. In the latter mode a long pulse is supplied to the MH0025. The input current is of the general shape as shown in Figure AI-6. I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50 to 60 mA). Q_1 will begin to turn-off when I_{IN} decays below V_{BE}/R_1 or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R_0 C_{IN}} \qquad \text{(AI-8)}$$

Where:

R_0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \frac{V_{BE}}{R_1}$ and solving for t_1 yields:

$$t_1 = R_0 C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R_0 C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-10)}$$

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200pF is:

$$t_{PW} \cong \frac{25ns + 150ns}{2} + (65\Omega)(2{,}200pF) \ln \frac{50mA}{2.5mA} = 517ns$$

A plot of pulse width for various types of drivers is shown in Figure AI-7. For applications in which

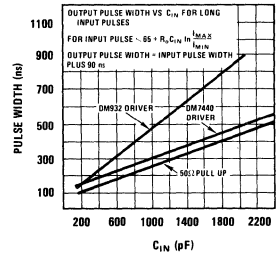

FIGURE AI-7. Output PW Controlled by C_{IN}

the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

The MH0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and plus 20V. The MH0025 is shown in Figure AI-8 driving the address or pre-charge line in the logically controlled mode.

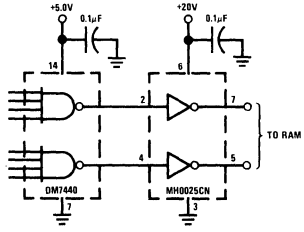

FIGURE AI-8. DC Coupled MH0025 Driving 1103 RAM.

If DC operation to a negative level is desired, a level translator such as the DM7800 or DH0034 may be employed as shown in Figure AI-9. Finally, the level shift may be accomplished using PNP transistors are shown in Figure AI-10.

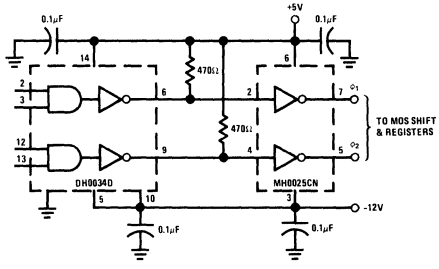

FIGURE AI-9. DC Coupled Clock Driver Using DH0034.

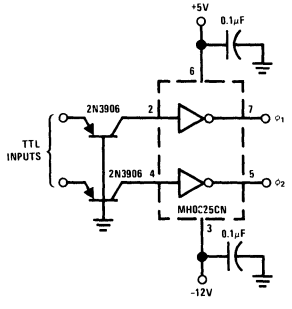

FIGURE AI-10. Transistor Coupled MH0025 Clock Driver.

APPENDIX II

MH0026 Circuit Operation

The schematic of the MH0026 is shown in Figure AII-1. The device is typically AC coupled on the input and responds to input current as does the MH0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q_1, Q_2, Q_5, Q_6, and Q_7 are "OFF" allowing Q_3 and Q_4 to come "ON." R_6 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q_1 and Q_2 turning them "ON." Simultaneously, Q_3 and Q_4 are snapped "OFF." As the input voltage rises (to about 1.2V), Q_5 and Q_6 turn-on. Multiple emitter transistor Q_5 provides additional base drive to Q_1 and Q_2 assuring their complete and rapid turn-on. Since Q_3 and Q_4 were rapidly turned OFF minimal power supply current spiking will occur when Q_7 comes "ON."

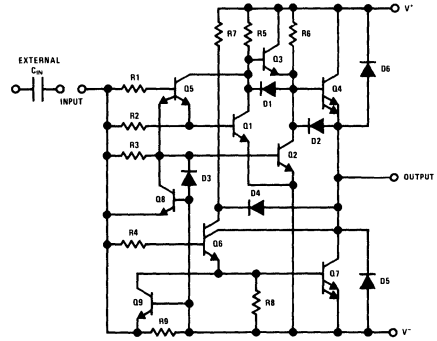

FIGURE AII-1. MH0025 Schematic (One-Half Circuit)

Q_6 now provides sufficient base drive to Q_7 to turn it "ON." The load capacitance is then rapidly discharged toward V^-. Diode D_4 affords a low impedance path to Q_6's collector which provides additional drive to the load through current gain of Q_7. Diodes D_1 and D_2 prevent avalanching Q_3's and Q_4's base-emitter junction as the collectors of Q_1 and Q_2 go negative. The output of the MH0026 continues negative stopping about 0.5V more positive than V^-.

When the TTL input returns to logic "0," the input voltage to the MH0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q_8 and Q_9 turn-on, pulling stored base charge out of Q_7 and Q_2 assuring their rapid turn-off. With Q_1, Q_2, Q_6 and Q_7 off, Darlington connected Q_3 and Q_4 turn-on and rapidly charge the load to within a V_{BE} of V^+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the MH0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\ \Delta V \qquad \text{(AII-1)}$$

For C_L = 1000pF, V^+ = 5.0V, V^- = -12V, $t_r \cong$ 21ns. Figure AII-2 shows MH0026 rise times vs. C_L.

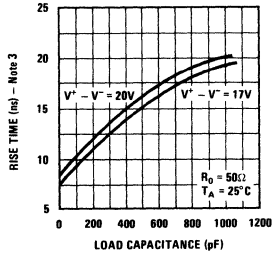

FIGURE AII-2. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the MH0026 is determined primarily by the capacitance Miller capacitance of Q_5 and Q_1 and R_5. The fall time may be predicted by:

$$t_f \cong (2.2)(R_5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q_3
= 2pF

$h_{FE}{}^2 = (h_{FEQ3}+1)(h_{FEQ4}+1)$
$\cong$ 500

For the values given and C_L = 1000pF, $t_f \cong$ 17.5ns. Figure AII-3 gives t_f for various values of C_L.

MH0026 Input Drive Requirements

The MH0026 was designed to be driven by standard 54/74 elements. The device's input characteristics

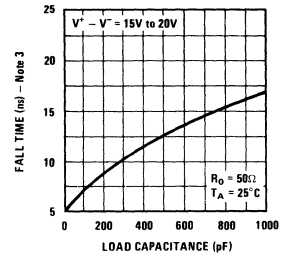

FIGURE AII-3. Fall Time vs Load Capacitance

are shown in Figure AII-4. There is breakpoint at $V_{IN} \cong$ 0.6V which corresponds to turn-on of Q_1 and Q_2. The input current then rises with a slope of about 600Ω ($R_2 \parallel R_3$) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q_5 and Q_6. The slope at this point is about 150Ω ($R_1 \parallel R_2 \parallel R_3 \parallel R_4$).

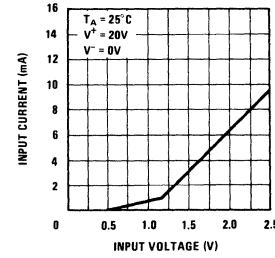

FIGURE AII-4. Input Current vs Input Voltage

The current demanded by the input is in the 5 to 10mA region. A standard 54/74 gate can source currents in excess of 20mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a MH0026. As far as the MH0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the MH0025 and MH0026 is that the MH0026 requires that the output pulse width be logically controlled. In short, the input pulse width $\cong$ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the MH0026 "ON." As before:

$$t_1 = R_0 C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AII-3)}$$

or

$$C_{IN} = \frac{t_1}{R_0 \ln \frac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

In this case R_0 equals the sum of the TTL gate output impedance plus the input impedance of the MH0026 (about 150Ω). I_{MIN} from Figure AII-5 is about 1mA. A standard 54/74 series gate has an high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20mA into 1.2V. For an output pulse width of 500ns,

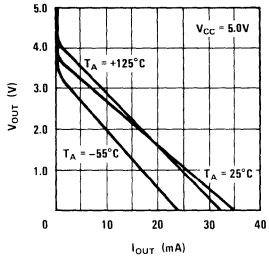

FIGURE AII-5. Logical "1" Output Voltage vs Source Current

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega)\ln \frac{20mA}{1mA}} = 560pF$$

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, MH0026, and temperature variations.

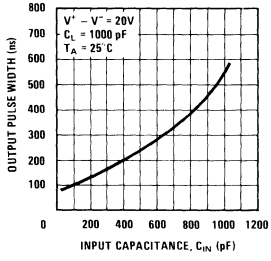

FIGURE AII-6. Optimum Input Capacitance vs Output Pulse Width

A plot of optimum value for C_{IN} vs desired output pulse width is shown in Figure AII-6.

DC Coupled Applications

The MH0026 may be applied in direct coupled applications. Figure AII-7 shows the device driving address or pre-charge lines on an MM1103 RAM.

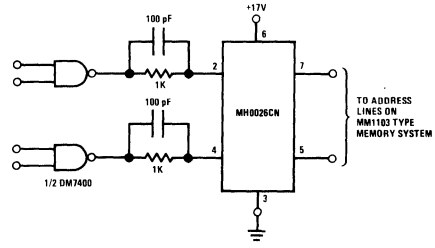

FIGURE AII-7. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a DC level shift, the circuit of Figure AII-8 or AII-9 are recommended.

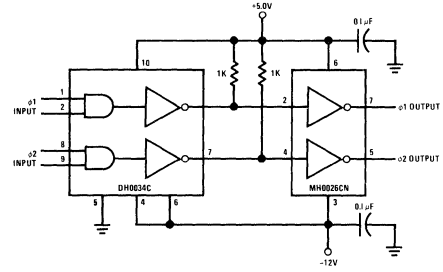

FIGURE AII-8. Transistor Coupled MOS Clock Driver

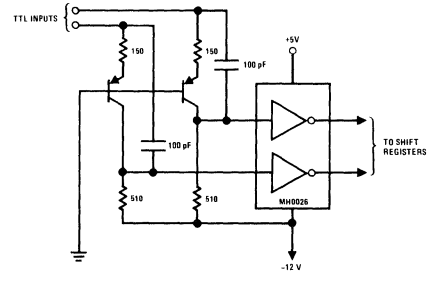

FIGURE AII-9. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007 Direct coupled, single phase, TTL compatible clock driver.

MH0009 Two phase, direct or AC coupled clock driver.

MH0012 10MHz, single phase direct coupled clock driver.

MH0013 Two phase, AC coupled clock driver.

MH0025 Low cost, two phase clock driver.

MH0026 Low cost, two phase, high speed clock driver.

MH8808 Dual clock driver for MM5262 2k RAM.

MOS Oscillator/Clock Drivers

MH7803/MH7807 – Complete two phase clock system for MOS micro-processors and calculators.

MOS RAM Memory Address and Precharge Drivers

MH8804 Quad TTL to 1103 address driver.

MH8805 Dual TTL to 1103 address driver.

MH0025 Dual address and precharge driver.

MH0026 Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034 Dual high speed TTL to negative level converter.

DM7800 Dual TTL to negative level converter.

DM7810/DM7812/DM7819 – Open collector TTL to positive high level MOS converter gates.

DM78L12 Active pull-up TTL to positive high level MOS converter gates.

MOS to TTL Level Converters and Sense Amps

DM7802/DM7806* – Dual sense amp for MM5262 2k MOS RAM memory.

LM165 Series* – Hex sense amp MOS to TTL.

LM163/LM75107/LM75207* – Dual sense amp for MM1103 1k MOS RAM memory.

Voltage Regulators for MOS Systems

LM109/LM140 Series – Positive regulators.

LM120 Series – Negative regulators.

LM125 Series* – Dual +/– regulators.

*To be announced.