Data Sheet

Count display ic ZN1040E

RS stock numbers 306-285

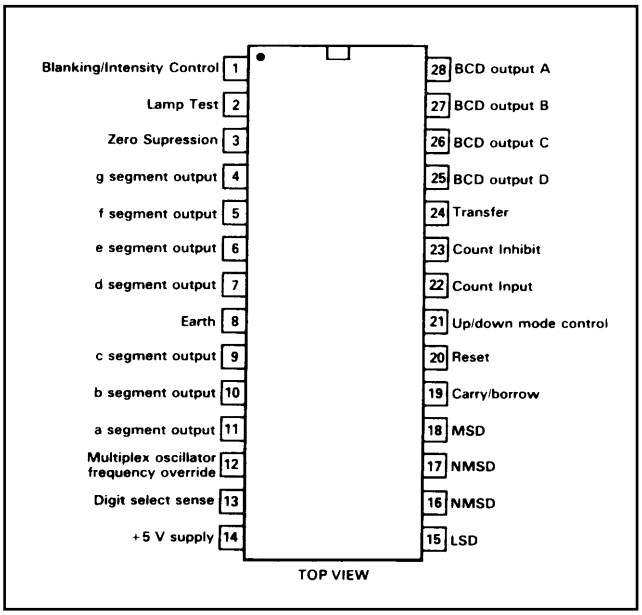
The ZN1040 is designed to satisfy the need for a universal count/display circuit suitable for the widest possible range of applications. The bipolar device allows fast count rates and high output currents to drive seven -segment LED displays, whilst BCD outputs allow interfacing to decoders for other types of display. Contained in a 28 dual-in-line package it requires a supply of 5 volts and consumes an internal current of 90mA typical.

Absolute maximum ratings

Supply voltage _____ 5.5 Volts
Segment output currents_____ 100mA
Other output currents _____ 25mA
Operating temperature range _____ –20˚C to 70˚C
Storage temperature range _____ –55˚C to 125˚C

Features

- 4 decade synchronous up/down counter with memory
- Carry/borrow output for direct synchronous cascading
- BCD and seven-segment outputs
- Segment outputs can drive LED displays directly
- Schmitt trigger on count input for slow input waveforms
- Count inhibit gating
- Full 5V compatibility, both on supply and TTL compatible interface.



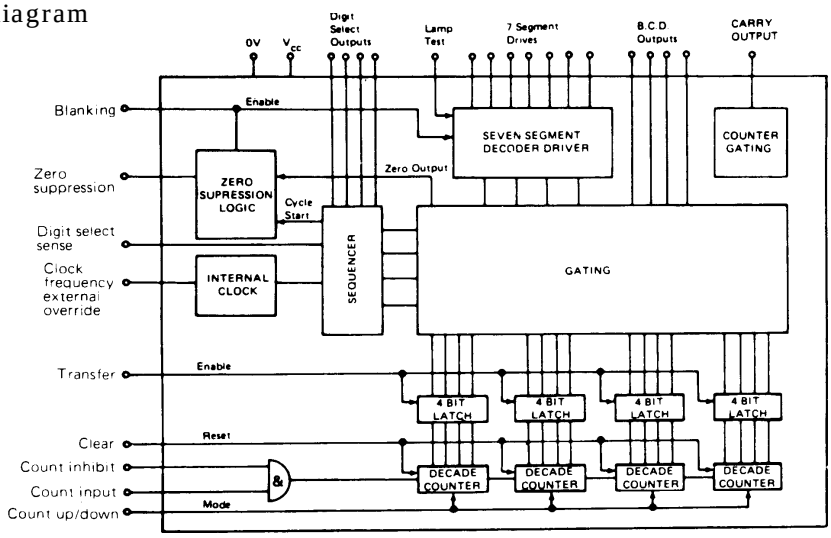
Electrical characteristics (at 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Count input positive going threshold	V_T+	-	1.5	-	V	
Count input negative going threshold	V_T-	-	1	-	V	
Input logic 1	V_{IH}	2	-	-	V	
Input logic 0	V_{IL}	-	-	0.8	V	
High level input current	I_{IH}	-	-	20	µA	
Low level input current	I_{IL}	-	-	–600	µA	
Carry and BCD output logic 1		2.4	3.3	-	V	^{1}Load = 0.4mA
Digit select output logic 1	V_{OH}	2.4	3.3	-	V	^{1}Load = -0.4 mA
Output logic 0 (except segments)		-	0.25	0.5	V	^{1}Load = 16mA
Segment output logic 0		-	0.3	0.6	V	^{1}Load = 50mA
Maximum count rate		5	8	-	MHz	
Transfer pulse width	50		-	-	ns	
Clear pulse width	100		-	-	ns	
Supply voltage	V_{CC}	4.75	-	5.25	V	
Supply current	I_S	-	90	-	mA	

Notes:

1. Digit select outputs may be made to operate in either direction. If digit select sense terminal is at logic 1, the digit select outputs go high to access and vice versa.
2. Inputs source 0.6mA maximum when at logic 0 and sink 20μA maximum when at logic 1.
3. The count input feeds into a Schmitt trigger possessing approximately 0.6 volt hysteresis. The inhibit control must not be altered while the count is at logic 1. The up/down control may, however, be altered asynchronously from count due to internal latching, but this only changes the mode when the count input is at logic 1.
4. When zero suppression (pin 3) is tied to ground the zero blanking function is disabled; i.e. zero's in MSD's will be displayed.
5. The clock terminal frequency is normally left open circuit, free running at about 500kHz. Alteration of the frequency is affected by adding an external capacitor between the clock frequency terminal and earth (pins 12 and 8). The rate may also be determined externally by overriding the internal clock with a TTL drive onto the clock frequency terminal.
6. Output logic 0 (not segments) is normally under 0.4V as for TTL and only rises when segments and other outputs are loaded with worst case conditions.
7. Unused inputs should be connected via a 1kΩ resistor to supply, in conformity with standard TTL practice.
8. A common anode LED display may show slight 'ghosting' due to the turn-off time of the PNP anode access transistors. This can be virtually eliminated by slowing down the scan rate with a suitable external capacitor from pin 12 to ground such as a 1000pF or 0.01μF.
9. The inhibit and count inputs must not be tied together when using more than four digits.

Figure 1 System diagram



Pinning details

Pin No.	Logic level to operate	Function	Pin No.	Logic level to operate	Function
1	0 to blank	Blanking/intensity Control	15		*LSD - Digit select output
2	0	Lamp test	16		
3	1	Zero suppression	17		*NMSD - Digit
4	0	g segment output	18		select output
5	0	f segment output	19	1 when 9999 and up. or when 0000 and down and when count at 0	Carry/borrow
6	0	e segment output	20	'0' to reset	Reset
7	0	d segment output	21	1 'up' 0 'down'	Up/down mode control
8	N/A	Earth	22	0 to 1 transition	Count input
9	0	c segment output	23	'0' to inhabit	Count inhabit
10	0	b segment output	24	'0' to hold	Transfer
11	0	a segment output	25	TTL levels	BCD output D
12	TTL drive pulses	Multiplex oscillator frequency override	26	TTL levels	BCD output C
13	1 (+ve pulses) 0 (–ve pulses)	Digit select sense	27	TTL levels	BCD output B
14	N/A	+ 5 volts supply	28	TTL levels	BCD output A

*LSD - Least significant digit
NMSD - Next most significant digit.

Operating notes
Section 1 : Counter

Counter operation

The counter section of the ZN1040E is a synchronous four decade BCD counter. Each decade consists of four flip-flops which are clocked simultaneously on the positive going edge of the count input pulse. Suitable steering logic ensures that the 16 flip-flops count in a four decade BCD sequence. The BCD outputs of the counter are connected to data latches in which the count may be stored for subsequent decoding and display.

The counter and count control circuitry are shown in Figure 2 whilst the input and inhibit input circuits are shown in more detail in Figure 3.

Figure 2 **Count system functional diagram**

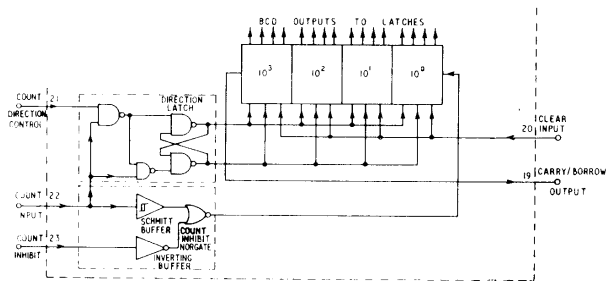
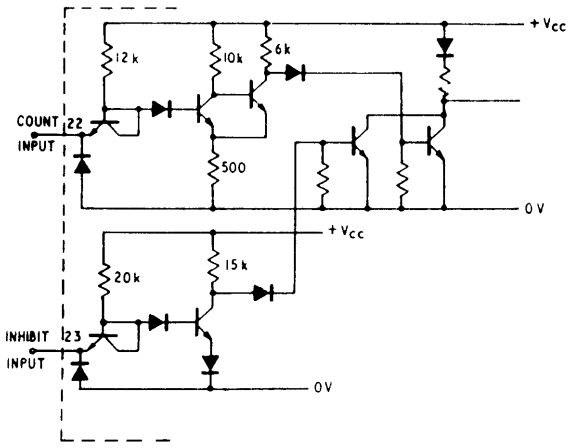


Figure 3 **Count input and inhibit circuit**

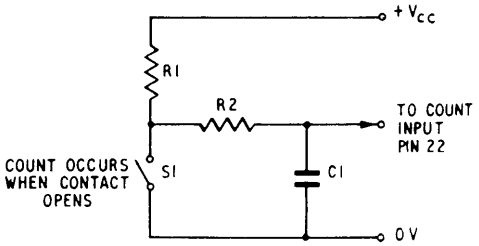


Counting occurs on the positive going edge of the count input pulse.

The counter input consists of a Schmitt trigger which allows the counter to operate reliably from input waveforms with very slow edges. It also allows a very simple anti-bounce circuit to be used when the count input is taken from a mechanical contact as shown in Figure 4.

Bounce occurs mainly on contact closure. R_2 is made very mush smaller than R_1 so that when the contact closes C_1 discharges rapidly to below the lower threshold of the Schmitt trigger. However, if the contact subsequently opens due to bounce, the time constant (R_1 + R_2) C_1 is of sufficient length so that C_1 does not charge to the upper threshold of the Schmitt trigger. When the contact genuinely opens then C_1 will charge and the counter will be clocked. The values of R_1, R_2 and C_1 will depend on the contact characteristics and the maximum count rate.

Figure 4 **Anti bounce circuit**



Inhibit input

The inhibit input is used to gate the count input pulses. When the inhibit input is high then the second input of the inhibit NOR gate is low and count pulses are allowed through, However, when the inhibit input is taken low, the second input of the inhibit NOR gate is taken high. This holds the output low so that the count pulses are blocked. Correct timing of the inhibit control is important. If the inhibit control is taken low when the count input is low then an extra positive going edge will be fed through the inhibit NOR gate and an extra count will result as shown in Figure 5a. The inhibit input should thus be operated when the count input is already high as shown in Figure 5b. If the count input waveform has a duty cycle which is not 50% then it is advisable to arrange that it is normally high, as in Figure 5b, since this makes operation of the inhibit control simpler.

Figure 5a **Incorrect inhibit operation**

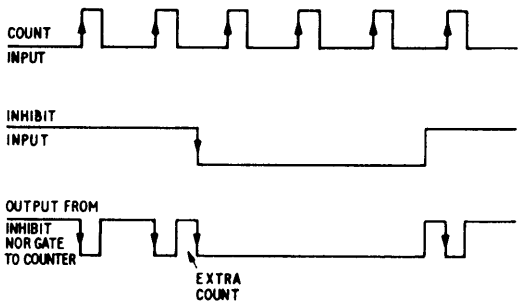
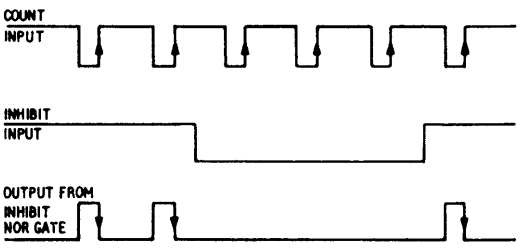


Figure 5b **Correct inhibit operation**



Direction control

Count direction is controlled by a 'D' latch (see counter operation) which can be set, for counting up, by taking the mode input high and reset, for counting down, by taking the mode input low. The clock input of this latch is connected to the count input and the state of the latch may therefore be changed only when the count input is high. If the count direction is to be reversed at a particular count then the state of the direction latch must be changed immediately that count is reached, whilst the count input is still high. Waiting until the count input has gone low again will result in the count direction not being reversed until the count input has gone high again, by which time an additional count will have been made in the original direction. Incorrect and correct operation of the direction control is illustrated in Figures 6a and 6b.

Figure 6a Incorrect operation of direction control

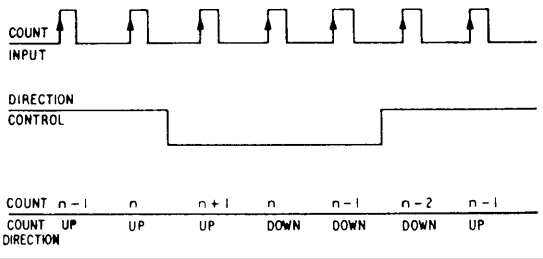
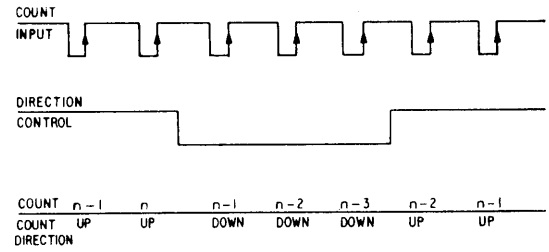


Figure 6b Correct operation of direction control



Counter reset

The counter may be reset to zero at any time by taking the clear input low. The counter will remain reset until the clear input is taken high again.

Care must be taken to set the direction latch to the correct state immediately after switch-on, otherwise the initial count may be made in the wrong direction. This may occur if the count input is low at switch-on since the direction latch may then set in either state. It is therefore advisable to ensure that the count input is normally high so that the direction latch will be set to the correct state at switch-on by the count direction control.

Carry/Borrow output

The carry/borrow output (pin19) may be used as an overflow indicator or to facilitate direct cascading of ZN 1040Es. When the count direction is UP then the carry output will go high on the next low-going edge of the count input after a count of 999 is reached. The carry output will go low again on the next high-going edge at the count input, when the count changes to 0000.

When the ZN 1040E is in the count DOWN mode then the carry output will go high on the next low-going edge at the count input after the counter reaches 0000. The carry output will go low again on the next high-going edge at the count input, when the count changes to 9999. In either case the carry output is subject to a propagation delay, t_c of typically 75ns, relative to the count input edges,

Carry output timing for both up ad down counting is shown in Figures 7a and 7b.

Figure 7a Carry output timing for up count

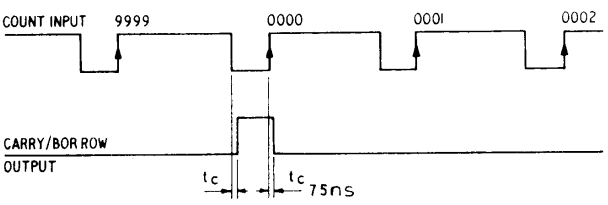
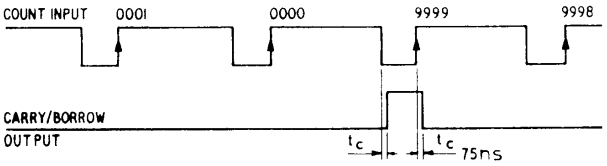


Figure 7b Carry output timing for down count



Count memory

Display latch

Each of the decode counters in the ZN1040E produces a binary coded decimal (BCD) number synchronous with the control input. The counter outputs are connected to the inputs of data latches which can store the counter outputs for subsequent display. Whilst the transfer input (pin 24) is high the latches are transparent, and their outputs will follow the data present at the inputs. When the transfer input is taken low the input data present at that instant will be held in the latches and will be unaffected by subsequent changes in the counter outputs.

Display multiplexing

Multiplex system

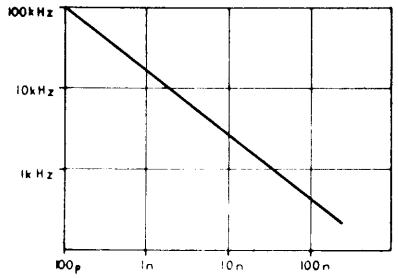
In order to economise on pin connections to the ZN 1040E, and to simplify connection to displays the outputs of the ZN 1040E are multiplexed, i.e. the four BCD output digits from the data latches are connected, one at a time, to a common data bus. The multiplexed BCD data is connected to four output pins directly and also is a BCD seven-segment decoder driver so that multiplexed seven-segment outputs are also available. Four digit select outputs indicate which digit is present on the BCD or 7-segment outputs at a particular time.

Internal multiplex oscillator

Clock pulses for the multiplex sequence are generated by an internal oscillator circuit. A capacitor of nominally 5pF is charged via a nominal 700k resistor to the upper threshold voltage of the Schmitt trigger. The nominal frequency of the multiplex oscillator is 500kHz but this can be altered by adding an external capacitor

between pin 12 and ground (Figure 8).

Figure 8 Nominal MPX oscillator frequency v. external capacitance



External MPX oscillator

Since the Schmitt trigger input of the MPX oscillator is only coupled to three fairly high impedances (10k and 700k resistors, and a 5pF capacitor) it is a simple matter to override the oscillator action by driving pin 12 from a low impedance external source such as a normal TTL output. Taking pin 12 high will hold the MPX oscillator output high, whilst taking pin 12 low will hold the output low. In this was the multiplexed BCD outputs of the ZN1040E can be synchronised to an external clock. This can be useful if, for example, the BCD output data is to be compared, digit by digit, with some preset limit. In this case the MPX frequency must at least be four times the input frequency to ensure that each digit has been compared before the next input pulse arrives.

The MPX input can be overdriven at frequencies up to 1MHz which means that the BCD outputs can be compared at count frequencies up to 250kHz.

Multiplex sequence generation

The output of the MPX oscillator is connected to the clock input of a sequence generator which is essentially a four-stage ring counter. This produces a sequence of four output pulses which are used to gate the BCD outputs, in sequence, on to four output lines.

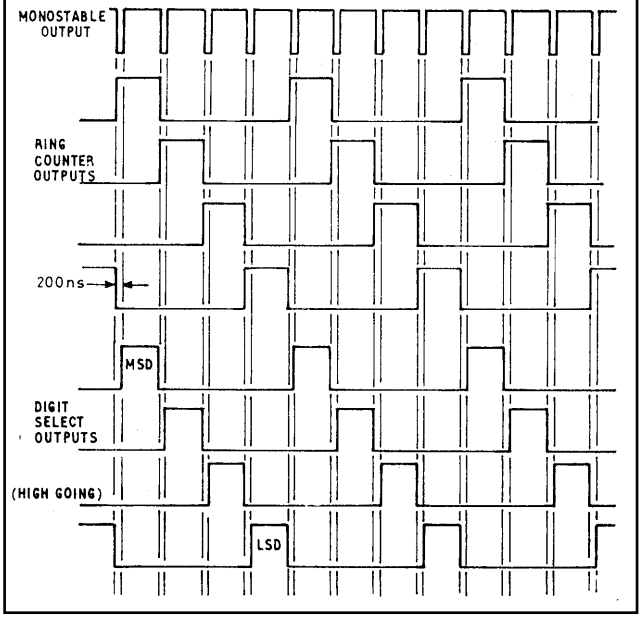
Digit select output circuit

Gating allows the selection of either high-going or low-going digit select pulses, thus allowing either common-anode or common-cathode displays to be driven using simple circuits. When the digit select sense input (pin 13) is high then the digit select pulses are high-going, when this input (pin 13) is low the digit select pulses are low-going. A timing diagram for high-going digit select pulses is given in Figure 9. For low-going pulses the digit select waveforms are simply inverted.

Seven-segment outputs

The seven segment outputs (pins 4-7, 9-11) are active low and can sink at least 50mA. The segment cathodes of common-anode displays may thus be driven directly.

Figure 9 Digit select output circuit

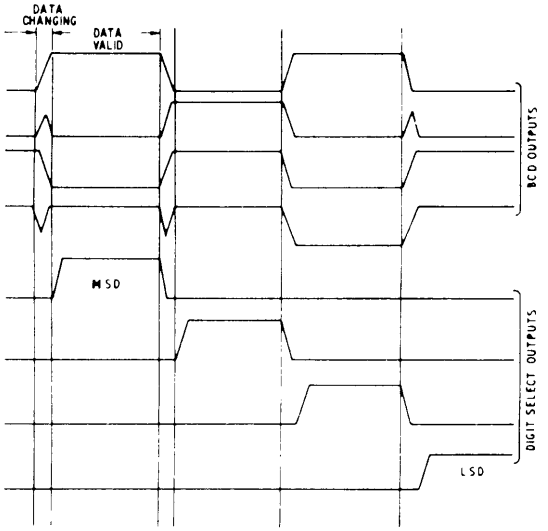


BCD outputs

The BCD output for each digit appears on the BCD output lines synchronous which the appropriate digit select pulse. However, since the MPX sequence gating is driven directly from the ring counter outputs, there is no inter-digit gap between one set of BCD data and the next. During the transition between digits the BCD data must therefore be considered invalid. If the BCD data is to be utilised (eg. stored in an external latch or compared) then the simplest was to overcome this problem is to make use of the leading edge of the digit select pulse to indicate when the data is valid. This is illustrated in Figure 10.

Similar comments also apply to the seven-segment outputs, but since these are normally used only for display driving, the problem does not usually arise.

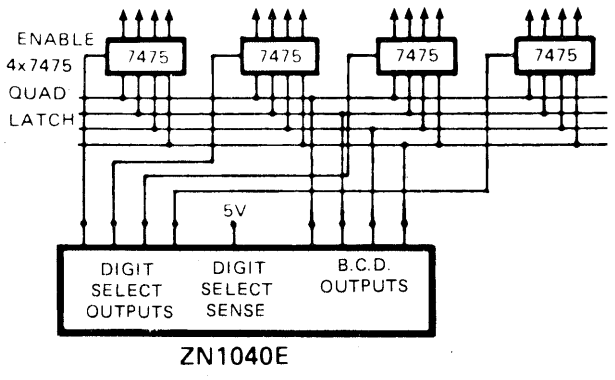
Figure 10 BCD output timing



Providing parallel BCD outputs

If outputs are required in parallel form rather than series parallel form the arrangement of Figure 11 may be used. A 7475 may be used as the digit select outputs are arranged to occur only while BCD outputs of the ZN1040E are stationary.

Figure 11 ZN1040E providing parallel BCD outputs



Zero suppression, blanking, decimal point and lamp test

The ZN1040E provides automatic blanking of leading zeros in the display, thus improving readability. A decimal point input is also provided which allows leading zeros to be displayed where these occur after the decimal point. A blanking input is provided to inhibit the display together with a lamp test input to check the operation of all display segments.

Blanking

Operation of the blanking input is extremely simple. When this input is high the seven-segment decoder functions normally and when this input is taken low the output of AND gate N6 goes low and the seven segment transistors are all turned off, blanking the display.

Zero blanking

Zero blanking operates on the principle of leaving the display blanked until non-zero data is detected at the outputs of the digit select gates. The trailing edge of the LSD output of the ring counter triggers a monostable which sets flip-flop N4/N5. The output of N4 holds one input of N6 low and the display is therefore blanked. It remains blanked until a non-zero digit appears on the BCD data bus, thus taking one or more of the inputs of NOR gate N3 high. The output of N3 then goes low resetting flip-flop N4/N5 so that the leading non-zero digit and all subsequent digits are displayed.

Should all four digits be zero then the flip-flop will be reset when the LSD output of the ring counter goes high and the output of N1 goes low. This ensures that the right hand digit (LSD) is always displayed, even if zero.

DP input

If not used, the decimal point input is normally held high. If a decimal point is used in the display then the DP input can be utilised to prevent the possibility of a blanked digit appearing after the decimal point. This is achieved by feeding a low-going pulse into the DP input synchronously with the digit select pulse for the digit where the decimal point is to appear. This resets flip-flops N4/N5 so that the display is unblanked for this digit and all subsequent digits even if there are leading zeros after the decimal point. Depending on whether the display has left or right-hand decimal points the display will be of the form .0 ----- or 0. -----. If there is to be a decimal point before the MSD then left-hand point displays must obviously be used. If no leading zero blanking is required then the DP input is simply grounded, when all digits will be displayed.

A timing diagram for the DP input is shown in Figure 9. It should be pointed out that the ZN1040E does not produce an output to drive the decimal point of display, this must be done externally.

Lamp test

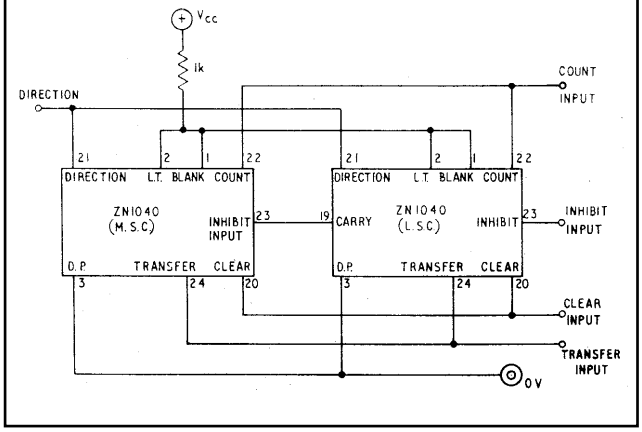
Operation of the lamp test function is quite simple. Taking the lamp test input low applies the BCD code 1000 (8) to the inputs of the BCD seven-segment decoder/driver. Simultaneously flip-flop N4/N5 is reset via N2 and N3, the output of N6 goes high, the display is unblanked and displays 8888. The blanking input must be high for lamp test to operate as a low blanking input will override the lamp test input and blank the display.

Applications information

Cascading the ZN1040E

If a count greater than 4 digits is required then two ZN1040Es may be cascaded using the carry/borrow output; or additional TTL decade counters may be added. To cascade two ZN1040s the carry/borrow output of the less significant counter is connected to the inhibit input of the more significant counter and the count inputs are linked as shown in Figure 12. The MCS is thus inhibited until after the 9999th clock pulse when the inhibit input will be taken high by the carry output of the LSC. On the leading edge of the 1000th clock pulse the MSC count will increase by 1 whilst the LSC count will go to zero. After the carry propagation delay the carry output of the LSC will go low and the MSC will again be inhibited. A timing diagram for this sequence of events is shown in Figure 13.

Figure 12 Cascading ZN1040Es without leading zero blanking



The leading zero blanking facility of the ZN1040E cannot be used directly in this application since the blanking circuits would operate independently for each device, leading to gaps in the display when the count was 999 or less, eg. ---0 -456.

This problem can be overcome by grounding the DP inputs of both counters this inhibiting the zero blanking, or alternatively the DP input of the LSC may be grounded giving zero blanking only on the first three digits of the MSC.

When ZN1040Es are cascaded then separate display interfacing will be used for each set of four digits.

Figure 13 Timing diagram for cascaded ZN1040Es

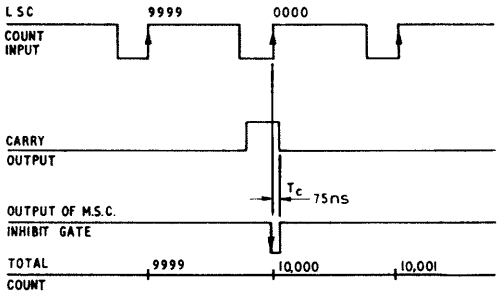
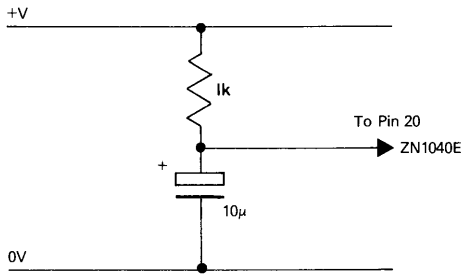


Figure 14 Power on reset circuit if required



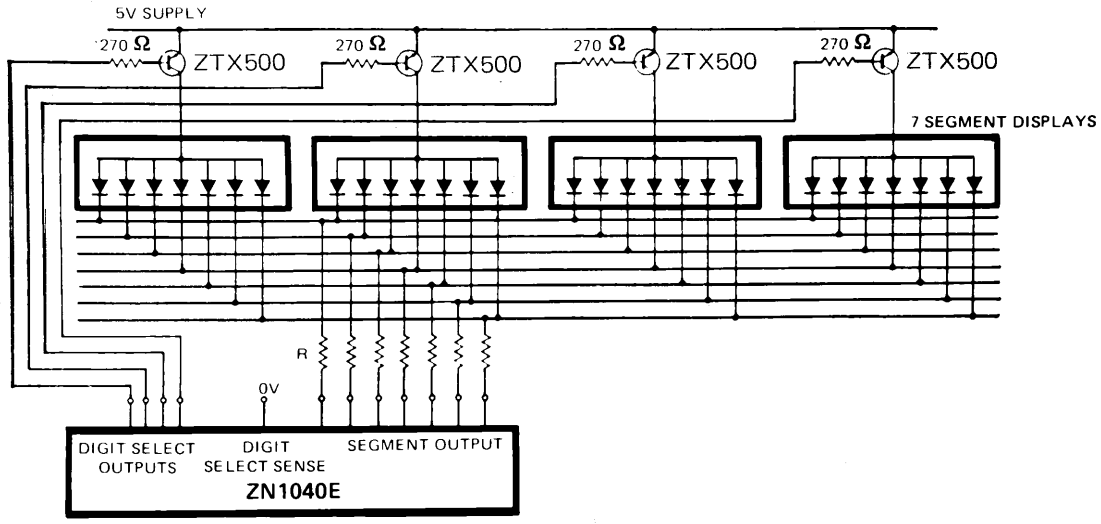
Display interfacing

The ZN1040E is versatile and able to drive virtually any display with minimal buffering. The detailed circuitry for popular types of display is described below. Good supply decoupling close to the IC is recommended, together with extra capacitance to slow down the scan rate to 10kHz or less. An internal 'pull up' resistor on the chip obviates the use of an external resistor when driving into displays requiring PNP transistors.

a) Common anode LED displays

The circuit shown below, contains 4 low power PNP transistors and 11 resistors. As a guide, for 0.3in displays, Resistor 'R' should be approximately 100Ω.

Figure 15 ZN1040E driving common anode LED displays



b) Common cathode LED displays

For common cathode use, 11 transistors and 18 resistors are required. The value of 'R' remains as shown in Figure 15.

Figure 16 ZN1040E driving common cathode LED displays

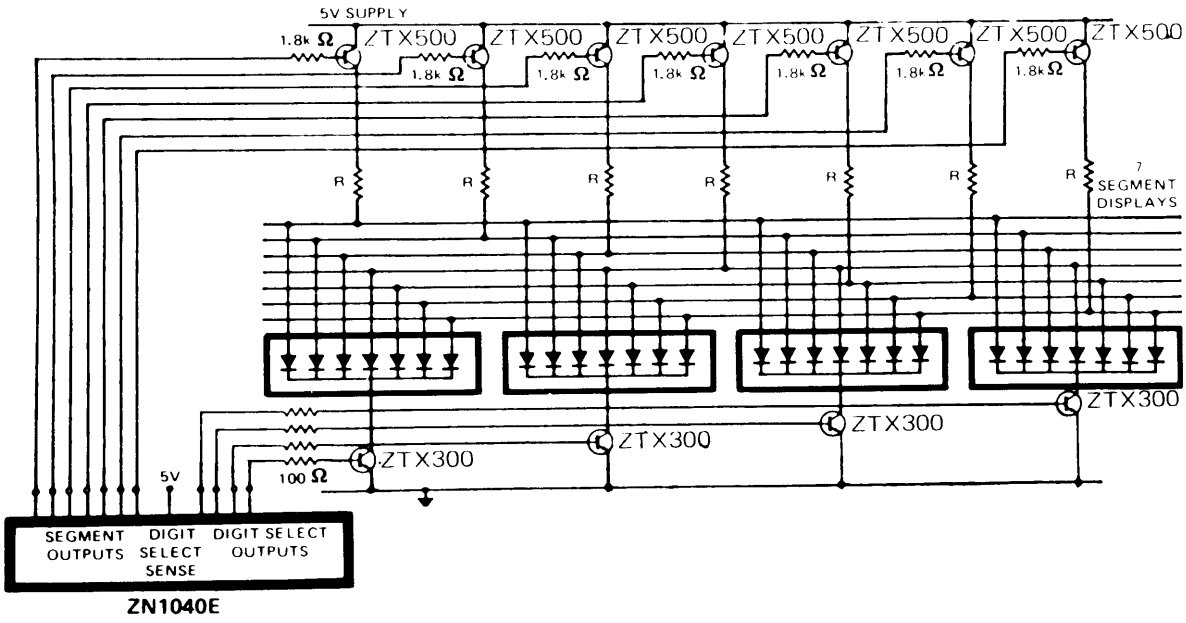
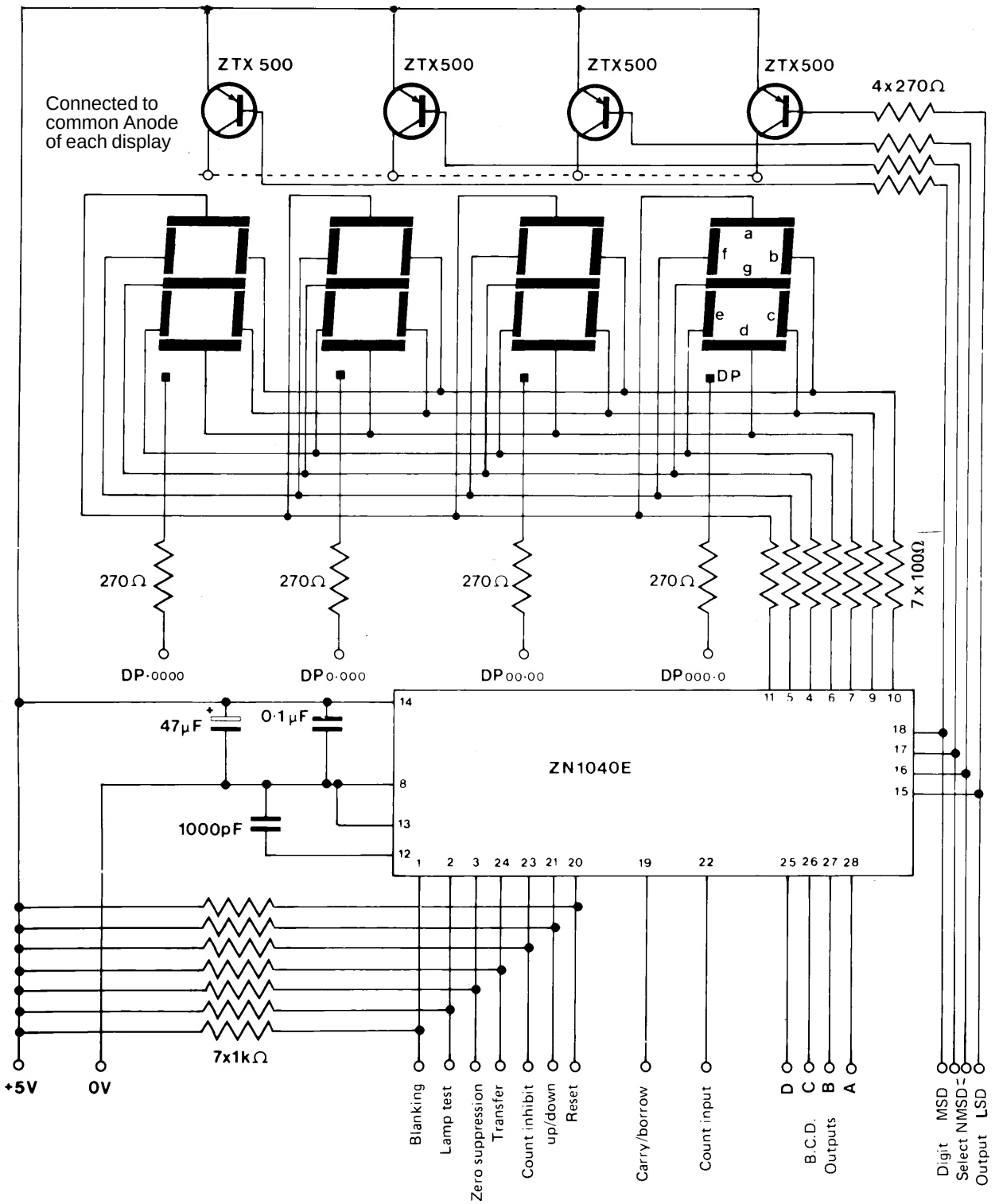


Figure 17 Full circuit driving four common anode displays



Printed circuit board 434-239 available.

Recommended components;
47µF 16v Tantalum 102-724
0.1µF 30v Disc ceramic 124-178
1000pF 100v Monolithic ceramic 125-676

All resistors 0.25W high stability carbon film.
7 segment display 0.3in 587-894 (Red) or 587-901 (Green).

RS Components, PO Box 99, Corby, Northants, NN17 9RS
Telephone: 01536 201234
An Electrocomponents Company